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**A MEMS Floating Element Shear Stress Sensor
for Hypersonic Flows**

**Final Report for
Phase I of STTR Contract # F49620-03-C-0114
For Performance Period 10/1/03 – 7/29/04**

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1 Overview

This report describes the results of a nine-month effort to develop a proof of concept, high-bandwidth, high-resolution, silicon micromachined piezoresistive floating element shear-stress sensor for the measurement of unsteady hypersonic flow phenomena. The work focused on three parts: (1) modeling, optimization, and fabrication of a piezoresistive-based micromachined, floating element shear stress sensor, (2) modeling, fabrication, and testing of an optical geometric Moiré interferometry-based floating element sensor, and (3) test facility development and characterization.

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3 Piezoresistive Floating Element Shear Stress Sensor

This section summarizes the development of a robust, high-bandwidth, high-resolution, silicon micromachined piezoresistive floating element shear-stress sensor possessing through-wafer backside electrical contacts for unsteady hypersonic flow measurement applications. During the past nine months, we have developed a comprehensive nonlinear electromechanical model of the sensor. This model was then leveraged to obtain optimal sensor designs for several specification sets associated with various candidate hypersonic flow phenomena. In parallel with these efforts, a microfabrication process flow for the sensor was synthesized. Once the sensor design and process flow tasks were completed, a microfabrication mask set was generated and microfabrication initiated.

3.1 Sensor Modeling

Floating-element sensors directly measure the integrated force produced by the wall shear stress on a flush-mounted movable "floating" element. The floating element is attached to either a displacement transducer or is part of a feedback force-rebalance configuration. A schematic of a generic MEMS floating element structure is given in Figure 3-1. The floating element possesses a length, L_e , width W_e and thickness t . The floating element is suspended over a recessed gap g by silicon tethers that also serve as restoring springs. The floating element is attached to either a displacement transducer or is part of a feedback force-rebalance configuration.

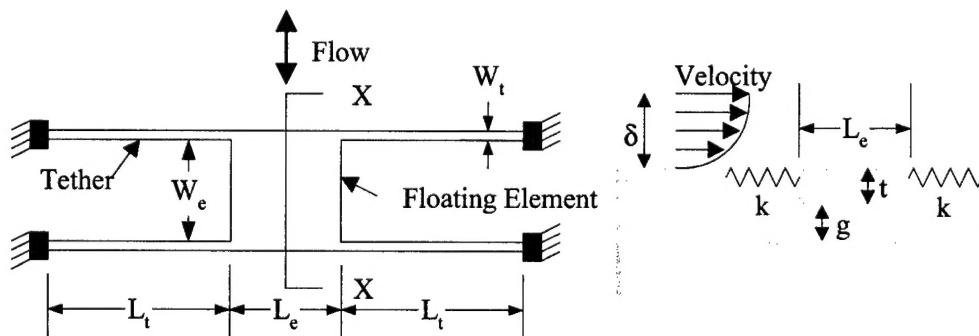


Figure 3-1: Schematic plan view and cross-section of a typical floating-element sensor.

The first micromachined floating element sensor structure developed in this effort integrates side-implanted diffused resistors into the element tethers for piezoresistive detection. Figure 3-2 shows a cut-away top view schematic of the floating element, sidewall implanted p-type silicon piezoresistors, the heavily doped end-cap region, and polysilicon through-wafer interconnects. In this transduction scheme, the integrated force produced by the wall shear stress on the floating element causes the tethers to deform and thus creates a mechanical stress field in the tethers. The piezoresistor responds to the mechanical stress field with a change in resistance from its nominal

unstressed value. The conversion of the shear-stress induced resistance change into an electrical voltage is accomplished by configuring the piezoresistors into a fully-active Wheatstone bridge.

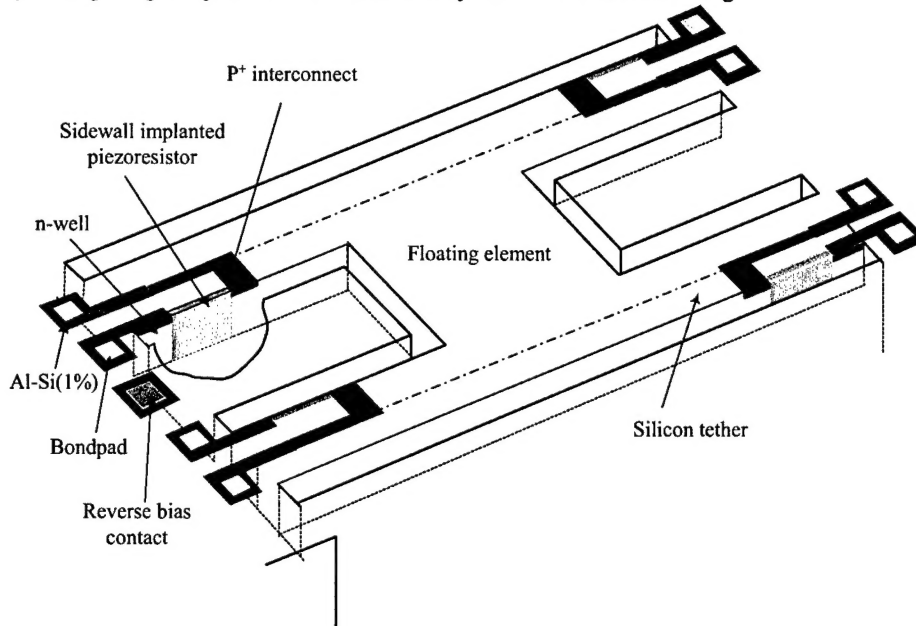


Figure 3-2: A schematic representation of the side-implanted floating element sensor.

The mechanical sensitivity, bandwidth and linearity of the shear stress sensor are directly related to the structural behavior of the device. For a piezoresistive sensor, the behavior of the stress or strain field in the tethers as a function of loading is of particular importance. In particular, the limitation of linearity for the difference between the wall shear stress τ_w and the tether bending stress σ_x , dictates the geometry of the device, while the stress field determines piezoresistor placement. Therefore, the modeling of the electromechanical transducer consists of two parts. First, the lateral displacement of the sensor and the stress field in the tethers must be related to the wall shear stress. Second, the stress field must be related to a change in resistance.

3.1.1 Quasi-Static Mechanical Modeling

Assuming that the floating element moves rigidly under the applied shear stress, the tethers can be modeled as clamped-clamped beams of length $2L_t$, width W_t and thickness T_t , subjected to a distributed load Q (per unit length) and a central point load P as shown in Figure 3-3. The distributed load is the direct effect of shear stress acting on the tethers and is given as $Q = \tau_w W_t$, where τ_w is the shear stress. The point load is the effect of the resultant force on the floating element and is equal to $P = \frac{1}{2} \tau_w W_e L_e$. The factor of half comes from a pair of clamped-clamped beams.

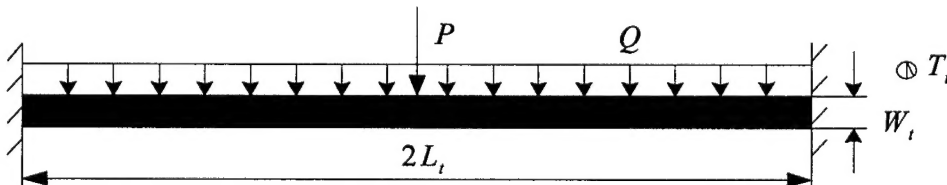


Figure 3-3: Simplified clamped-clamped beam model.

Using Euler-Bernoulli or small deflection beam theory, the deflection of the beam is

$$w(x) = \frac{-\tau_w}{4EW_t^3T_t} \left[(3W_eL_eL_t + 8W_tLT_t^2)x^2 - (2W_eL_e + 8W_tL_t)x^3 + 2W_t x^4 \right] \quad (0 \leq x \leq L_t), \quad (1)$$

where E is the Young's modulus of silicon. The maximum deflection occurs at the center of the beam ($x = L_t$) and corresponds to the floating element displacement

$$\delta_L = \frac{\tau_w W_e L_e}{4ET_t} \left[\frac{L_t}{W_t} \right]^3 \left[1 + 2 \frac{W_t L_t}{W_e L_e} \right], \quad (2)$$

Euler-Bernoulli beam theory assumes small deflections such that the strain at the neutral axis of the beam can be neglected. For sufficiently large shear stresses applied to a device, this theory will fail. These limits are important because device linearity is required to preserve spectral fidelity for time-resolved measurements and is therefore used as a constraint during optimization. Large deflection theory provides insight into the variation of maximum linear shear stress as a function material properties and geometry. We pursued three different analysis techniques to determine the non-linear mechanical behavior of the sensor: an energy based method, an exact analytical method and a finite element analysis (FEA) using *CoventorWare*®. The maximum deflection is at the center of the beam ($x = L_t$), and the deflection predicted by the strain energy method is

$$\delta_{NL} \left[1 + \left(\frac{3}{4} \right) \left(\frac{\delta_{NL}}{W_t} \right)^2 \right] = \frac{\tau_w W_e L_e}{4ET_t} \left[\frac{L_t}{W_t} \right]^3 \left[1 + 2 \frac{W_t L_t}{W_e L_e} \right]. \quad (3)$$

Therefore, the mechanical response of the floating element sensor will be linear provided that the displacement of the sensor is small in comparison to the tether width, $(\delta/W_t)^2 \ll 1$. The three models were compared for a representative structure given in Table 3-1. Figure 3-4 illustrates the agreement between the three nonlinear models for the representative structure.

Table 3-1: The material properties and geometry parameters for a representative structure used verify the mechanical models.

Density of the material ρ_{Si} (kg/m ³)	2330
Young's modulus E (GPa)	168
Poisson ratio ν	0.27
Length of tethers L_t (μm)	400
Thickness of the tethers T_t (μm)	3
Width of the tethers W_t (μm)	4
Length of the square floating element L_e (μm)	150

The corresponding stress distribution using Euler-Bernoulli beam theory through the width of the tether is given by

$$\sigma_x(x, y) = -\frac{\tau_w W_e L_e L_t}{W_t^2 T_t} \left(1 - \frac{2y}{W_t} \right) \left[\left(\frac{3}{4} + \frac{2W_t L_t}{W_e L_e} \right) - \left(\frac{3}{2} + \frac{6W_t L_t}{W_e L_e} \right) \left(\frac{x}{L_t} \right) + \frac{3W_t L_t}{W_e L_e} \left(\frac{x}{L_t} \right)^2 \right] \quad (0 \leq x \leq L_t), \quad (4)$$

where $y=0$ is at the surface of the beam. As shown in Figure 3-5, the analytical stress distribution given in Equation (4) is in excellent agreement with a FEA model for the representative structure given in Table 3-1.

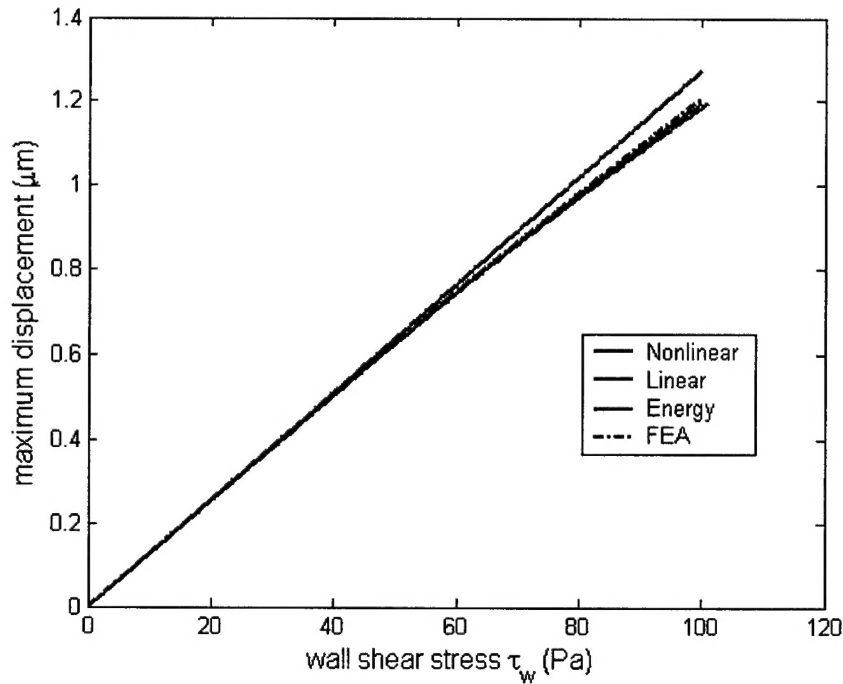


Figure 3-4: Representative results of the mechanical response for representative structure given in Table 3-1. The maximum displacement of the sensor (in microns) is plotted as a function of applied shear stress. Equation (3) (Energy) is in excellent agreement with the exact nonlinear (Nonlinear) solution and the finite element analysis (FEA). Note that the small deflection theory, Equation (2), (linear) over predicts the deflection for a given applied shear stress.

3.1.2 Dynamic Response

The dynamic response of the shear stress sensors have been explored by combining the fundamental structural model presented in Section 3.1.1 with a lumped-element energy model. This model provides a compact analytical description of the multi-energy domain transducer and was used to provide insight into the scaling of the dynamic response. The main assumption with lumped element modeling (LEM) is that the frequencies of interest in all of the energy domains are sufficiently low such that the quasi-static assumption is valid.¹ This enables the distributed system to be “lumped” into idealized discrete circuit elements. Under this approximation, the structural dynamics equations are replaced by equivalent Kirchoff’s laws for velocity u and shear force F .

From a LEM perspective, the two sets of tethers are modeled an effective spring possessing a stiffness k . This stiffness shares a common displacement with the effective mass m of the tethers and floating element as well as the dissipation (or damper) R of the system. Therefore, the sensor is modeled as a spring-dashpot system or a capacitor (compliance of the spring)-inductor (representing mass)-resistor (representing the damper) as schematically shown in Figure 3-6. This model is valid the first resonance frequency of the system, which is appropriate for design purposes.

Based on the equivalent circuit shown in Figure 3-6, the frequency response function of the device is

$$H(j\omega) = \frac{x(j\omega)}{F(j\omega)} = \frac{1}{(j\omega)^2 m + j\omega R + k}, \quad (5)$$

¹ Rossi, M., *Acoustics and Electroacoustics*. 1988, Norwood, MA: Artech House.

where ω is the angular frequency, $x = \delta$ is the element displacement and $j = \sqrt{-1}$. Assuming a lightly damped system, the first resonant frequency f_r of the sensor is

$$f_r = \frac{1}{2\pi\sqrt{Cm}}, \quad (6)$$

where C is the effective mechanical compliance of the beam and m is the effective mass of the tethers and beam.

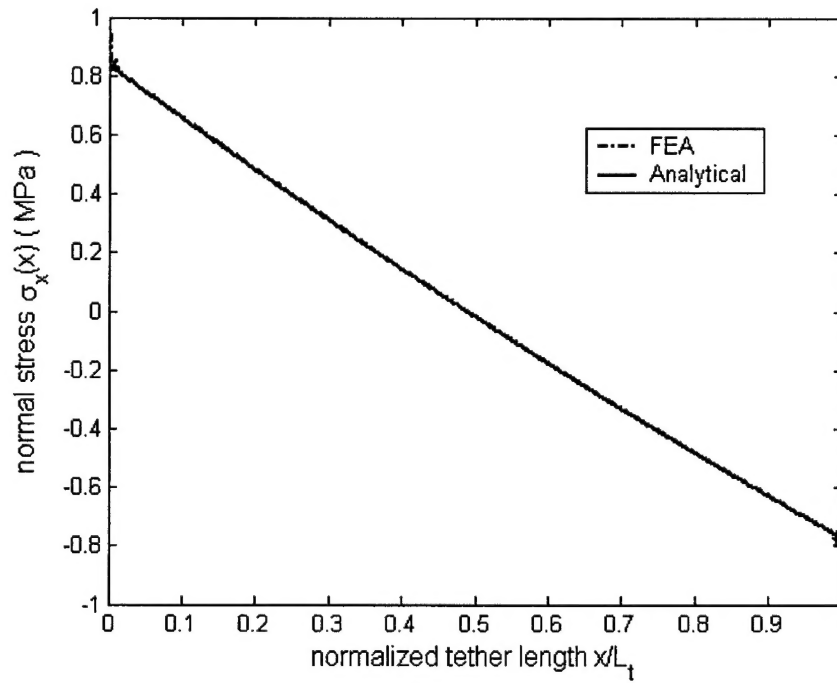


Figure 3-5: Representative results verifying the analytical stress profile given in Equation (4) for $y=0$ against FEA for the representative structure given in Table 3-1 for $\tau_w = 5 \text{ Pa}$.

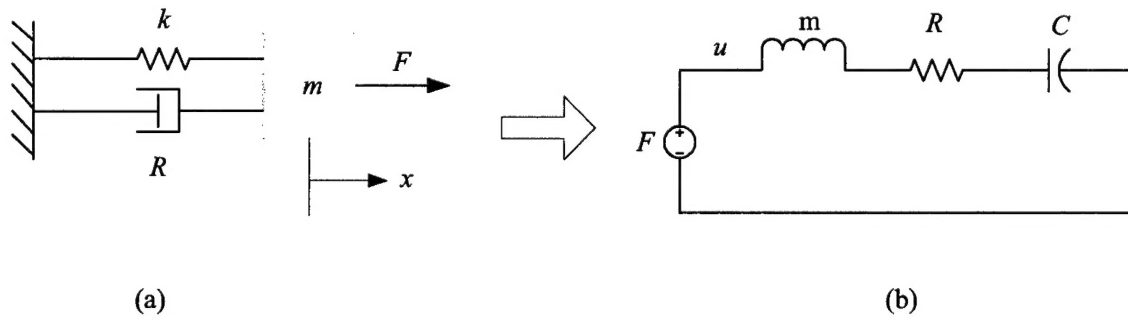


Figure 3-6: Lumped element model of floating element sensor: (a) spring-mass-dashpot system and (b) equivalent circuit.

The effective mechanical compliance is determined by equating the potential energy stored in the beam to that of an equivalent lumped system,

$$C_{mc} = \frac{-w(0)^2}{2EI \int_0^{L_t} \left(\frac{d^2 w(x)}{dx^2} \right)^2 dx} \quad (7)$$

The effective mass is obtained by equating kinetic energy of the sensor to that of the equivalent lumped model.

$$m = \rho L_e W_e T_e + 2 \frac{\rho_{si} W_t T_t}{w^2(0)} \int_0^{L_t} w^2(x) dx, \quad (8)$$

where ρ_{si} is the density of silicon and $w(x)$ is given by Equation (1). Representative results verifying the lumped element model via FEA are given in Table 3-2. In general, LEM predicted the first resonant frequency of the device to within 5%.

Table 3-2: Representative results of the resonant frequency and effective mass predicted by LEM and FEA for the representative structure given in Table 3-1.

	Effective mass (kg)	Frequency (kHz)
LEM	1.66e-10	12.44
FEA	1.72e-10	12.47

3.1.3 Piezoresistive Transduction

For the piezoresistive device, the floating element sensor structure integrates side-implanted diffused resistors into the element tethers for piezoresistive detection. In this transduction scheme, the integrated force produced by the wall shear stress on the floating element causes the tethers to deform and thus creates a mechanical stress field in the tethers. The piezoresistor responds to the mechanical stress field with a change in resistance from its nominal unstressed value according to the piezoresistive sensitivity,

$$\frac{\Delta \rho}{\rho} = \frac{\Delta R}{R} = \pi_l \sigma_l, \quad (9)$$

where ρ is the resistivity of the resistor, R is the resistance, Δ signifies the perturbation in the resistance or resistivity due to the piezoresistive effect, σ_l is the normal stress along the beam, and π_l is the longitudinal piezoresistance coefficient. The value of π_l for silicon is a function of 3 fundamental piezoresistance coefficients, $\pi_{11}, \pi_{12}, \pi_{44}$,

$$\pi_l = \pi_{11} - 2(\pi_{11} - \pi_{12} - \pi_{44})(l_1^2 m_1^2 + m_1^2 n_1^2 + n_1^2 l_1^2), \quad (10)$$

where (l_1, m_1, n_1) is the set of direction cosines between the longitudinal direction and the crystal axis. The fundamental piezoresistance coefficients depend on crystal orientation, doping type and level, and temperature. Are typically expressed as a product of their lightly-doped room temperature value and piezoresistive factor $P(N, T)$

$$\pi(N, T) = \pi_0 P(N, T), \quad (11)$$

where N is the dopant impurity concentration and T is the temperature. Smith² has experimentally determined the values of piezoresistive coefficients for low doping levels and therefore represents the maximum coefficient. The

² Smith, C.S., *Piezoresistance Effects in Germanium and Silicon*. Physical Review, 1954. **94**(42-49).

longitudinal and transverse piezoresistance coefficients π_l and π_t in $\langle 110 \rangle$ direction for n-type and p-type silicon are given in Table 3-3. For a $\langle 100 \rangle$ wafer, the maximum piezoresistance coefficient for p-type silicon occurs in the $\langle 110 \rangle$ direction, while for n-type silicon the maximum is in the $\langle 100 \rangle$ direction with a larger magnitude than p-type silicon. As shown in Table 3-4, p-type silicon is more sensitive than n-type silicon in the $\langle 110 \rangle$ direction. For this transducer design, we will use p-type silicon piezoresistors and align our resistors in the $\langle 110 \rangle$ direction to maximize the piezoresistive sensitivity.

Table 3-3: Piezoresistive coefficients π_0 for n-type and p-type silicon.

	$\pi_{11} (10^{-11} \text{Pa}^{-1})$	$\pi_{12} (10^{-11} \text{Pa}^{-1})$	$\pi_{44} (10^{-11} \text{Pa}^{-1})$
n-type	-102.2	53.4	-13.6
p-type	6.6	-1.1	138.1

Table 3-4: Piezoresistive coefficients for p-type and p-type silicon in $\langle 110 \rangle$ direction on the $\langle 100 \rangle$ plane.

	$\pi_l (*10^{-11} \text{Pa}^{-1})$	$\pi_t (*10^{-11} \text{Pa}^{-1})$
n-type	-31.2	-17.6
p-type	71.8	-66.3

Many models have been developed in an attempt to predict the relationship between piezoresistive factor $P(N, T)$. Kanda's³ model is the most popular and is accurate at a low concentration, but it under predicts the roll-off of $P(N, T)$ with increasing concentration for $N > 10^{17} \text{ cm}^{-3}$ when compared to experimental data. For this project, we use the experimental fit by Harley and Kenny⁴ as shown in Figure 3-7

$$P(N, T) = 0.2014 \log \left(\frac{1.53 \times 10^{22}}{N} \right). \quad (12)$$

In general, it is desirable to use the higher doping concentration consistent despite the lower piezoresistance coefficient because it results in a lower impedance resistor possessing reduced susceptibility to electromagnetic interference, lower Johnson noise and the large carrier numbers induce lower $1/f$ noise. In addition, the temperature dependence of the piezoresistance coefficient is reduced significantly as the concentration increases. Particularly, when the concentration is above 10^{20} cm^{-3} , the piezoresistance coefficient becomes almost independent of the temperature variation. However, the sensitivity will degrade due to the reduced piezoresistance coefficient π_l , so there is a tradeoff between sensitivity and noise floor.

For the structure shown in Figure 3-2, the side-implanted piezoresistors are fabricated by first implanting a p-type impurity (boron) which is then followed by a drive-in step. The impurities diffuse vertically and produce an impurity concentration profile that decreases from the surface to the junction depth. If the unstrained impurity profile, as a function of depth $N(y)$, is known, the piezoresistive profile $\pi(y)$ can be determined. As shown in Equation (4), the stress varies along the beam and across the depth y_j of the piezoresistor. Therefore, the product of the stress and the piezoresistance coefficient distributions need to be integrated in the electromechanical model. As per Equation (9), both the unperturbed R and perturbed ΔR values of the resistance must be calculated.

³ Kanda, Y., *A Graphical Representation of the Piezoresistive Coefficients in Silicon*. IEEE Trans. Electron Devices, 1982. **ED-29**(64): p. 64-70.

⁴ Harley, J.A. and T.W. Kenny, *1/f Noise Considerations for the Design and Process Optimization of Piezoresistive Cantilevers*. J. Micro Elec. Mech. Sys., 2000. **Vol.9**(No.9).

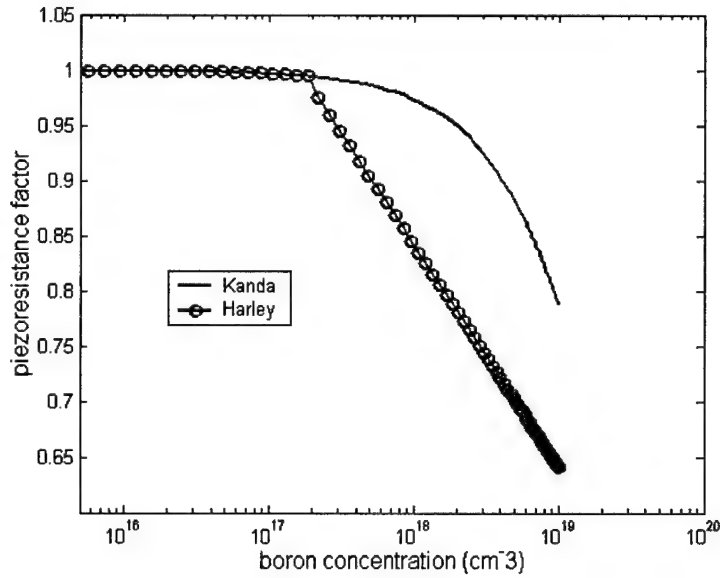


Figure 3-7: Piezoresistive factor as a function of impurity concentration for *p*-type silicon at 300 K .

where $\rho_{eo}(y)$ is the unstressed resistivity. For the non-uniform doping, the unstrained resistivity $\rho_{eo}(y)$ is

$$\rho_{eo}(y) = \frac{1}{\mu_p(y)qN(y)}, \quad (13)$$

where the mobility $\mu_p(y)$ can be obtained by Nishida & Sah's model⁵.

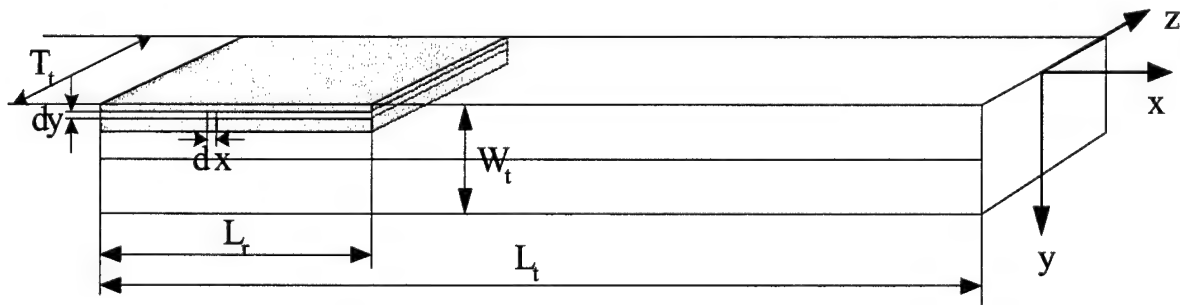


Figure 3-8: Schematic illustrating relevant geometric parameters for piezoresistive sensitivity calculation.

The resistance of each vertical slice is summed in series, giving the resistance of a full horizontal slice,

⁵ Nishida, T. and C.-T. Sah, *A Physical Based Mobility Model for MOSFET Numerical Simulation*. IEEE Transactions on Electron Devices, 1987. **ED-34**(No.2): p. 310-320.

$$R_{slice} = \int_{L_0}^{L_0+L_r} \frac{\rho_{eo}(y)dx}{T_i dy}. \quad (14)$$

When the beam is deflected, thus generating a stress field, the resistance in this slice varies as

$$\Delta(dR_{slice}) = \frac{\Delta\rho_{eo}(y)dx}{T_i dy}. \quad (15)$$

The piezoresistor responds to the mechanical stress field with a change in resistivity from its nominal unstressed value according to

$$\frac{\Delta\rho_{eo}}{\rho_{eo}} = \bar{\pi}_i \sigma_i, \quad (16)$$

where $\bar{\pi}_i$ is the conductance-weighted piezoresistive coefficient,

$$\bar{\pi}_i = \int_0^{y_j} \pi_i(y) \Sigma(y) dy / \int_0^{y_j} \Sigma(y) dy, \quad (17)$$

and $\Sigma(y) = 1/\rho(y)$ is the conductivity. Therefore, the change in resistance of the full slice is

$$\Delta R_{slice} = \int_{L_0}^{L_0+L_r} \frac{\rho_{eo}(y) \bar{\pi}_i \sigma_i dx}{T_i dy}. \quad (18)$$

For a single slice, the sensitivity is

$$\frac{\Delta R_{slice}}{R_{slice}} = \frac{\tau_w \bar{\pi}_i W_e L_e L_i}{W_i^2 T_i} \left[\left(\frac{3}{4} + \frac{2W_i L_i}{W_e L_e} \right) - \left(\frac{3}{4} + \frac{3W_i L_i}{W_e L_e} \right) \left(\frac{2L_0 + L_r}{L_i} \right) + \frac{W_i L_i}{W_e L_e} \frac{(L_0 + L_r)^2 + L_0(L_0 + L_r) + L_0^2}{L_i^2} \right] \left(1 - \frac{2y}{W_i} \right). \quad (19)$$

The maximum sensitivity occurs at the surface, $y = 0$,

$$\frac{\Delta R}{R_{surface}} = \frac{\tau_w \bar{\pi}_i W_e L_e L_i}{W_i^2 T_i} \left[\left(\frac{3}{4} + \frac{2W_i L_i}{W_e L_e} \right) - \left(\frac{3}{4} + \frac{3W_i L_i}{W_e L_e} \right) \left(\frac{2L_0 + L_r}{L_i} \right) + \frac{W_i L_i}{W_e L_e} \frac{(L_0 + L_r)^2 + L_0(L_0 + L_r) + L_0^2}{L_i^2} \right]. \quad (20)$$

If the junction depth y_j is small enough compared to the tether width, one can use the surface stress to approximately estimate the response. In practice, y_j is usually not negligibly small and the transverse impurity and stress profiles across the thickness must be accounted for in the sensitivity calculation.

To obtain the sensitivity for the entire piezoresistor, the contribution of each horizontal slice across the beam thickness needs to be summed. Since the resistance is in parallel, it is convenient to use conductance G to calculate the integration. Equation (9) is rewritten as

$$\Delta R/R = -\Delta G/G. \quad (21)$$

Therefore, the total conductance is

$$G = \int_0^{y_j} \frac{T_i dy}{\rho_{eo}(y) L_r} . \quad (22)$$

The total change in conductance is rewritten as

$$\Delta G = \int_0^{y_j} \frac{\tau_w \pi_i W_e L_e L_i}{W_i^2 T_i} \left[\left(\frac{3}{4} + \frac{2W_i L_i}{W_e L_e} \right) - \left(\frac{3}{4} + \frac{3W_i L_i}{W_e L_e} \right) \left(\frac{2L_0 + L_r}{L_i} \right) + \frac{W_i L_i (L_0 + L_r)^2 + L_0 (L_0 + L_r) + L_0^2}{L_i^2} \right] \frac{\left(1 - \frac{2y}{W_i} \right) T_i dy}{\rho_{eo}(y) L_r} . \quad (23)$$

Therefore, the total sensitivity is obtained by substituting Equations (22) and (23) in Equation (21) to yield

$$\frac{\Delta R}{R} = -\frac{\Delta R}{R_{surface}} \int_0^{y_j} \left(1 - \frac{2y}{W_i} \right) \Sigma(y) dy / \int_0^{y_j} \Sigma(y) dy . \quad (24)$$

Physically, the second term in Equation (24) is the conductance average of the depth effect of the sensitivity.

The piezoresistive shear stress sensor is designed such that each of the four piezoresistors is located on a single tether. The four piezoresistors in the shear stress sensor form a full Wheatstone bridge circuit as shown in Figure 3-9, which provides maximum sensitivity to a small change in resistance. In a balanced bridge, the output of the bridge is null when the mean resistances R in all four legs are equal. Ideally, common mode disturbances have no effect while differential disturbances are linearly converted into the bridge output. To achieve a differential signal from shear stress based deflections, the piezoresistors are oriented such that the resistance modulation in each resistor of a given leg is equal in magnitude, but of opposite sign. This configuration is realized by designing the piezoresistors to be equal in size and by positioning them such that resistors 1 and 3 experience compressive stress when the element deflects, while 2 and 4 experience tension stress. This is achieved by simply placing the resistors on opposite sides of the tether as shown in Figure 3-2. In this case, the resistances in the Wheatstone bridge in Figure 3-9 are $R_1 = R_3 = R - \Delta R$ and $R_2 = R_4 = R + \Delta R$. The output voltage V_o that for a given bias voltage V_b is

$$V_o = \left(\frac{R_4}{R_3 + R_4} - \frac{R_1}{R_1 + R_2} \right) V_b = \frac{\Delta R}{R} V_b . \quad (25)$$

The shear stress sensitivity of a piezoresistive sensor is defined as the change of output voltage per unit of applied shear stress and is given as

$$S_M = \frac{\partial V_o}{\partial \tau_w} \approx \frac{\Delta V_o}{\tau_w} . \quad (26)$$

3.1.4 Piezoresistor Noise Issues

The key contributors to the electronic noise of the piezoresistor are thermal noise and low frequency $1/f$ noise. Physical fluctuations of the diaphragm at equilibrium at a temperature, T , can result in random motion of the diaphragm; however, the contribution of thermo-mechanical displacement noise to the piezoresistor output noise has been shown to be much smaller than the electronic noise sources except at mechanical resonance⁶. In addition, Brownian motion of the floating element due to random scattering of gas molecules is also negligible for the mass of

⁶ Papila, M., Haftka, R., Nishida, T., and Sheplak, M., "Piezoresistive microphone design Pareto optimization: tradeoff between sensitivity and noise floor," AIAA Paper 2003-1632, presented at the 44th AIAA/ASME/ASCE/AHS Structures, Structural Dynamics, and Materials Conference, Norfolk, VA April 07-10, 2003

the element under consideration. Thus, the electronic noise is computed using the power spectral densities of thermal and low frequency noise.

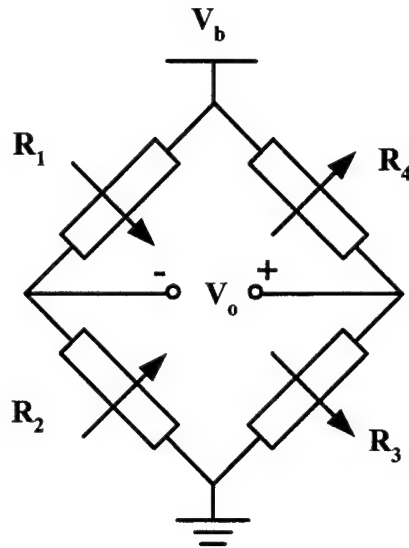


Figure 3-9: Schematic representation of general Wheatstone bridge.

Voltage fluctuations, at the external terminals of a resistor, are produced when electrons are scattered by the thermal vibrations of the lattice. These fluctuations are present in any device that dissipates energy due to thermal vibrations. Since higher temperatures lead to increased vibration motion, thermal noise power spectral density (PSD) is directly proportional to temperature. Moreover thermal noise PSD is independent of frequency since random thermal vibrations are not characterized by discrete time constants. The thermal noise PSD (S_{vT}) is given by⁷

$$S_{vT} = 4k_B T_K R, \quad (27)$$

where k_B is the Boltzmann constant, R is the resistance, and T_K is the temperature in Kelvin. In a piezoresistor, the r.m.s. noise voltage, E_{IR} , due to thermal noise is obtained by taking the square root of the thermal noise PSD integrated over the bin width of interest, $\Delta f = f_2 - f_1$,

$$E_{IR} = \sqrt{\int_{f_1}^{f_2} S_{vT} df} = \sqrt{4k_B T_K R \Delta f} \quad (28)$$

Piezoresistors also exhibit noise with a PSD that varies inversely with frequency when an external *dc* bias is applied. Since the PSD is more prevalent at lower frequencies, it is also known as low frequency noise. Two physical mechanisms have been proposed to account for the low frequency noise, random trapping/detrapping of carriers at surface and bulk electronic traps and random mobility fluctuations. Since the dominant mechanism may depend on the surface and electronic material properties, an empirical formulation is used to model the $1/f$ noise in the piezoresistors. Hooge's relation for $1/f$ noise PSD is given by⁸

⁷ Nyquist, H., *Thermal Agitation of Electric Charge in Conductors*. Phys. Rev., 1928. **32**: p. 110-113.

⁸ Hooge, F.N., *1/f Noise is No Surface Effect*. Phys. Lett.A, 1969. **29**: p. 139-140.

$$S_{v1/f} = \frac{\alpha_H V_b^2}{Nf} \quad (29)$$

where α_H , known as the Hooge's parameter which is an empirically obtained constant which ranges from 5×10^{-6} to 2×10^{-3} (we use $\alpha_H = 1 \times 10^{-3}$ for this research) and is sensitive to bulk crystalline silicon imperfections as well as to the interface quality. The r.m.s. noise voltage due to $1/f$ noise is obtained by integrating the noise PSD over the frequency range of operation,

$$E_{1/fR} = \sqrt{\frac{\alpha_H V^2}{N} \ln \frac{f_2}{f_1}} \quad (30)$$

Unlike the thermal noise, $1/f$ noise occurs under nonequilibrium conditions and is proportional to the applied voltage. From the inverse relation to the square root of the number of charge carriers, we see that $1/f$ noise increases in smaller volume and higher resistivity piezoresistors. A schematic illustration of a typical noise spectrum containing both thermal noise and low frequency $1/f$ noise is shown in Figure 3-10.

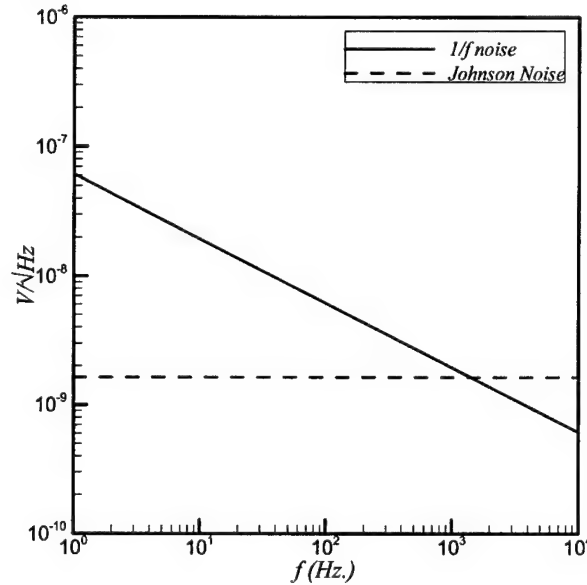


Figure 3-10: Schematic representation of a typical electronic noise spectrum containing both thermal noise and low frequency $1/f$ noise.

Assuming that the Wheatstone bridge is balanced, the total r.m.s. noise voltage V_N is

$$V_N = \sqrt{\frac{\alpha V_B^2}{4L_r T_i \int_0^{y_i} N(y) dy} \ln \left(\frac{f_2}{f_1} \right) + 4k_B T \cdot BWR}, \quad (31)$$

where the first term in the numerator is the contribution of Hooge noise and the second term is the contribution of Johnson noise. The minimum detectable shear stress τ_{\min} is the minimum shear stress at which the shear stress sensor can resolve in the presence of noise. It is defined as the ratio of noise floor to sensitivity

$$\tau_{\min} = \frac{V_N}{\Delta V_0 / \tau_{\max}}. \quad (32)$$

3.2 Sensor Design Optimization

To accurately measure turbulent shear-stress spectra, the measurement device must possess sufficient spatial and temporal resolution as well as high measurement resolution. Depending upon the candidate hypersonic flow phenomena and flow environment, these scales can vary by several orders of magnitude. This is also true for the dynamic range requirements of the device. In order to ensure relevance to the AFSOR program goals, we discussed several target specifications with leading hypersonic researchers. Specifically, conversations with Professor Lex Smits at Princeton University and Dr. Roger Kimmel at AFRL led to the choice of several sensor specifications for various candidate hypersonic flow phenomena as listed in Table 3-5.

For each of the six candidate designs, τ_{\max} is the maximum wall shear stress to be measured, f_{\min} is the minimum resonant frequency to provide adequate temporal resolution, L_{\max} is the maximum floating element size and is a spatial resolution constraint, while w_{\min} and t_i are the minimum tether width and thickness, respectively. The mechanical sensitivity, bandwidth and linearity of the shear stress sensor are directly related to the structural behavior of the device, while the minimum detectable shear stress value, τ_{\min} , is related to the electronic noise floor of the piezoresistors. Since both the sensitivity and noise performance metrics depend on the geometry of the piezoresistor, doping concentration and profile, and mechanical and electronic properties, the parameter design space for optimization is complex. For this problem, we used the minimum detectable shear stress as the objective function, subject to the geometrical constraints listed in Table 3-5.

Table 3-5: Candidate shear stress sensor specifications

Device #	1	2	3	4	5	6
$\tau_{\max} (Pa)$	50	50	100	100	500	500
$f_{\min} (kHz)$	10	50	50	100	100	300
$L_{\max} (\mu m)$	1000	1000	1000	500	500	500
$w_{\min} (\mu m)$	10	10	10	10	10	10
$t_i (\mu m)$	12	12	12	12	12	12

In addition to the geometric parameters, there are two other major factors involved in processing which affect sensitivity and noise: one is the depth y_j of the piezoresistor and the other is the surface doping concentration N_s . Choosing the depth of the piezoresistor represents a tradeoff between noise and sensitivity. If the doped layer y_j is very shallow, the number of carriers is small and the $1/f$ noise is high, but the piezoresistors is located in a region of maximum stress. Conversely, if y_j is very deep, the sensitivity will be reduced, but the impedance will also drop leading to associated reductions in electronic noise. The doping concentration affects the resistance value, the thermal and Hooke noise, and the sensitivity of the shear stress sensor. As shown in Figure 3-7, when the doping concentration increases, the piezoresistive coefficient π_l decreases. This has a direct impact on the sensitivity, as shown in Equation (23), although a higher concentration has more carriers for noise improvement. Besides piezoresistor depth and dopant concentration, annealing is also an important factor affecting sensitivity and noise. FLOOPS® is used to simulate the doping profile properly.

The constraints are determined by physical bounds, fabrication limits and performance requirements. The constraints used in this optimization and their associated physical explanations are listed as follows:

- Lower and upper bounds: $LB \leq L_i, W_i, T_i, L_r, V_B \leq UB$.
- Geometry of the piezoresistor: $0.1 \leq L_r/L_i \leq 0.4$

Since stress changes from compressive (tensile) to tensile (compressive) at the center of the tether, the sensitivity will be reduced if the length of the piezoresistor larger than $L_t/2$. To ensure low resistance contact with the piezoresistor, there is approximately a $10\mu m$ overlap at edge of the tethers. The length of the piezoresistor is limited, as follows,

- Resistance: $3 k\Omega \leq R \leq 5 k\Omega$

This represents a balance between the sensor resistance being an order of magnitude larger than the interconnect resistance, but small enough to minimize EMI.

- Frequency: $f_r \geq f_{\min}$

This depends on the specifications.

- Power consumption: $P_{ow} \leq 0.1 W$

When power, $P_{ow} = \frac{V_b^2}{R}$, increases to a large value the temperature of the piezoresistor will increase due to Joule heating, which results in voltage drift to due convective cooling as the device behaves in a manner similar to that of a thermal anemometer.

- Linearity: $\frac{|\delta_{NL} - \delta_L|}{\delta_{NL}} \leq 2\%$

This ensures that the mechanical sensitivity of the sensor remains linear at τ_{\max} . Equations (2)

and (3) are used to calculate δ_{NL} and δ_L .

Mathematically the optimization problem is expressed as

Minimize: τ_{\min}

Subject to:

$$LB \leq L_t, W_t, T_t, L_r, V_B \leq UB$$

$$0.1 \leq L_r/L_t \leq 0.4$$

$$3 k\Omega \leq R \leq 5 k\Omega$$

$$f_r \geq f_{\min}$$

$$P_{ow} \leq 0.1 W$$

$$\frac{\delta_{NL} - \delta_L}{\delta_{NL}} \leq 2\%$$

The optimization problem was implemented in MATLAB® using its optimization toolbox that employs sequential quadratic programming for non-linear constrained problems and calculates the gradients by finite difference method. The resulting optimal designs are shown in Table 3-6.

For each device, the optimal design indicated a dynamic range, which is defined as, $DR = 20 \log[\tau_{\max} / \tau_{\min}]$, in excess of 80 dB or over 4-orders of magnitude predicted measurement resolution.

Table 3-6: Optimal shear stress sensor designs for each case listed in Table 3-5.

Optimization Parameters	Device 1	Device 2	Device 3	Device 4	Device 5	Device 6
$L_t (\mu m)$	464.24	161.95	169.91	157.89	159.27	158.07
$W_t (\mu m)$	14	14.27	14.9677	14.4731	14.05	15.32
$T_t (\mu m)$	10	10	10	10	10	10
$W_e (\mu m)$	1000	1000	1000	500	500	188.04
$L_r (\mu m)$	62.95	63.13	63.09	63.15	63.06	63.17
$y_j (\mu m)$	0.5	0.5	0.5	0.5	0.5	0.5
$N_s (cm^{-3})$	1.0e+19	1.0e+19	1.0e+19	1.0e+19	1.0e+19	1.0e+19
$V_b (V)$	9.7	10	9.4	10	10	10
$P_{ov} (W)$	0.0170	0.0179	0.0159	0.0179	0.0179	0.0179
$f_r (kHz)$	10	50	50	105.89	100	300.19
$R (k\Omega)$	4.7189	4.7187	4.7188	4.7186	4.7189	4.7196
$S_M (V/Pa)$	6.07e-4	1.23e-004	1.16e-004	2.86e-5	3.09e-5	4.02e-6
$V_N (nV)$	134.88	138.39	130.49	138.36	138.47	138.31
$\tau_{min} (Pa)$	2.22e-4	0.0011	0.0011	0.0048	0.0045	0.0344
DR	107	93	99	86	101	83

3.3 Piezoresistive Sensor Fabrication

The first generation of the shear stress sensor is fabricated in an 8-mask, silicon-surface-micromachining process described in detail in the following sections. The 3D structure is schematically illustrated in Figure 3-2. The process starts with a 4-inch (100) n-type silicon-on-insulator (SOI) wafer with a 10 μm top silicon layer above a 2 μm buried silicon dioxide (BOX). Prior to initiating fabrication, several issues had to be resolved regarding the junction isolation of both the side-wall implanted piezoresistors and the piezoresistive contacts.

3.3.1 Microfabrication Process Flow

We have developed and simulated (using FLOOPS[®]) a microfabrication processes to realize a micromachined piezoresistive floating element shear-stress sensor possessing through-wafer backside electrical contacts. The process flow consists of a 10-mask microfabrication process containing 17 major steps. The details of the process flow are listed in APPENDIX A. The photo-masks have been designed using AutoCAD[®] and have been fabricated. The microfabrication process is currently ongoing as of the time of this report is currently on Step 11. An optical photograph of a partially fabricated device structure is shown in Figure 3-11. The estimated completion of the process is ~ 8/21/04.

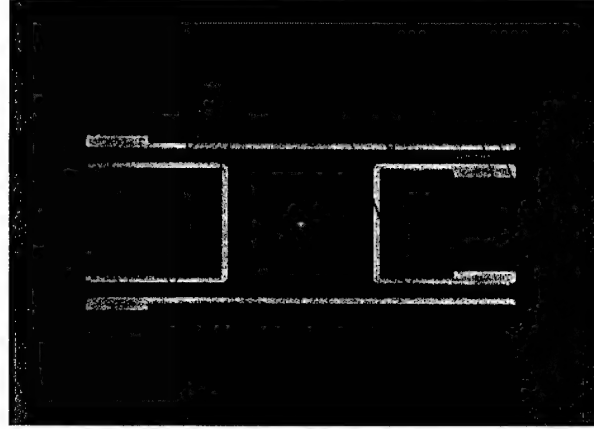


Figure 3-11: Optical photograph of a partially completed device (through step 10)

3.3.2 Junction Isolation Issues for Lateral Implants

One unexpected design issue that we discovered was the difficulty of developing junction isolated laterally diffused resistor in the sidewall of a tether. Without proper isolation, the piezoresistors will essentially be shorted to ground resulting in a non-functioning sensor. This issue had to be resolved prior to initiating the mask design.

The design issues involve a junction-isolated p-type piezoresistor and the p++ interconnects in an n-well, with a stress concentration at the edge of the tethers. As shown in Figure 3-12, the p-type piezoresistor, the p++ interconnect and the n-well all form P/N junctions. Three issues must be taken into account in the design: (1) maintaining junction isolation, (2) avoiding P/N junction breakdown while achieving the desired piezoresistor sensitivity, and (3) minimizing stress concentration on the edge of the tethers.

When a voltage is applied between the two p++ interconnects, the P/N junction voltage varies linearly with the position due to the linear voltage drop across a distributed resistance. For junction isolation, the P/N junction must be reverse-biased.

A P/N junction develops a space charge layer due to the depletion of carriers⁹. For uniform doping, the acceptor concentration in the P region is assumed to be N_A and the donor concentration in N region is assumed to be N_D . The space charge layer width on the p-side (x_p) and on the n-side (x_n) is given as a function of the junction voltage V_j :

$$x_p(V_j) = \left[\frac{2\epsilon_{Si}}{q} \frac{N_D}{N_A(N_A + N_D)} (V_{bi} - V_j) \right]^{1/2} \quad (33)$$

and

$$x_n(V_j) = \left[\frac{2\epsilon_{Si}}{q} \frac{N_A}{N_D(N_A + N_D)} (V_{bi} - V_j) \right]^{1/2}, \quad (34)$$

where $V_{bi} = \frac{kT}{q} \ln \left(\frac{N_A N_D}{n_i^2} \right)$ is the built-in voltage, $\epsilon_{Si} = 11.8 \times 8.854 \times 10^{-14} \text{ F/cm}$ is the silicon permittivity and $q = 1.602 \times 10^{-19} \text{ C}$ is the electric charge.

⁹ Plummer, J.D., M.D. Deal, and P.B. Griffin, *Silicon VLSI Technology*. Prentice Hall Electronics and VLSI Series, ed. C. Sodini. 2000: Prentice Hall.

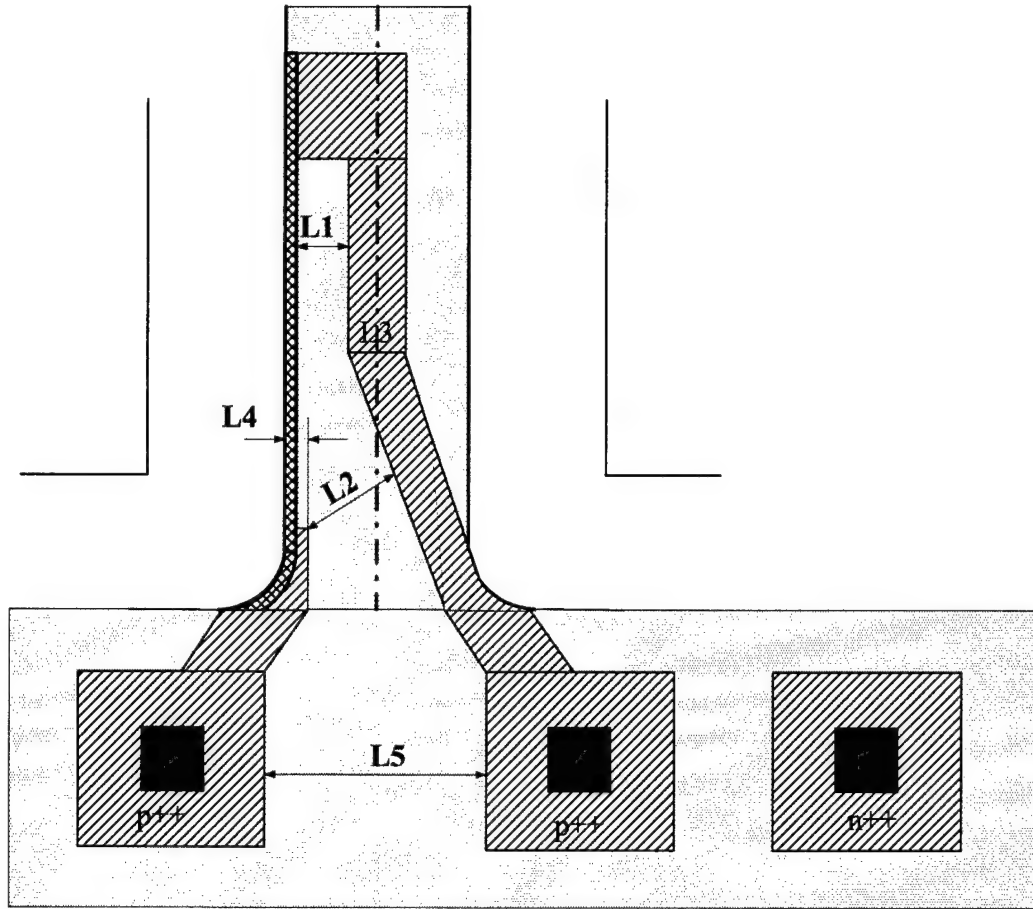


Figure 3-12 Top view schematic of the side-implanted piezoresistor and p++ interconnect in an n-well.

In order to electrically isolate the p++ regions, the entire length of the P/N junction must be reverse-biased ($V_j < 0$). However, the space charge layer width in the P and N region, x_p and x_n , increases with increasing reverse bias. The total space charge width $W(V_j)$ on the n-side is given by

$$W(V_j) = x_n(V_j) + x_n(V_B + V_j). \quad (35)$$

If $W(V_j)$ on the N side, increases to the width between the piezoresistor and the p++ interconnect, $L1$, or to the width between p++ interconnects, $L2$, the space charge layers will punch-through, causing the corresponding P regions to be shorted. To avoid punch-through, $W(V_j) \ll L1$ must be satisfied for all junction voltages V_j . Additional lateral diffusion must be taken into account considering the thermal budget. So the total isolation width is approximated by

$$W_{iso}(V_j) = 2L_d + x_n(V_j) + x_n(V_B + V_j) \quad (36)$$

where L_d is the lateral diffusion width that is estimated via Fig.4.10 in Jaeger. The total thermal budget $(Dt)_{tot}$ is equal to the sum of the Dt products for all high temperature cycles affecting the lateral diffusion, $(Dt)_{tot} = \sum D_i t_i$, where D_i and t_i are the diffusion coefficient and time associated with the processing step, respectively.

In this design, the doping profile is non-uniform and the acceptor concentration in the P region $N_A(y)$ and the donor concentration in the N region $N_D(y)$ vary with depth, as shown in Figure 3-13, which is based on the FLOOPS® simulation¹⁰. The cross view of the isolation width for a doping profile at a bias voltage of 10V is shown in Figure 3-14 and Figure 3-15, where the tether width is 14 μm . $L1$, $L2$, $L3$, $L4$ and $L5$ are set to 4 μm , 5 μm , 8.5 μm , 1.5 μm and 45 μm , respectively.

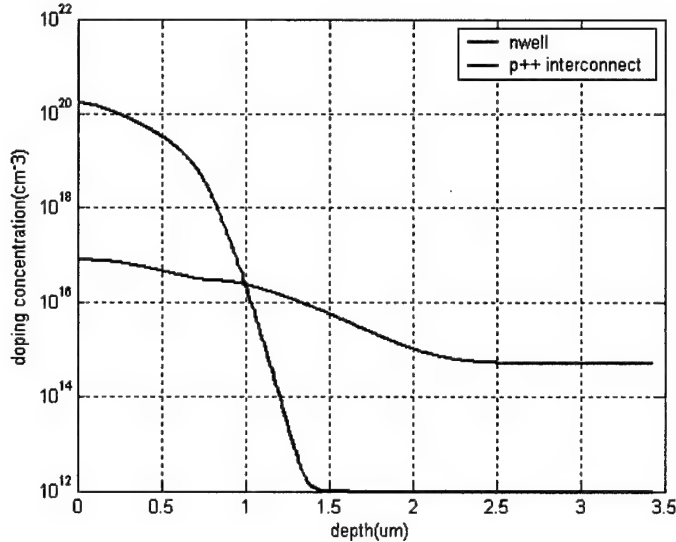


Figure 3-13 Simulated doping profile for n-well and p++ interconnect.

There is a tradeoff between the p++ interconnect width, $L3$ and $L4$, and the punch-through width, $L1$. $L3$ and $L4$ are desired to hold a large value in order to reduce the lead resistance, however, the tight space may cause P/N junction punch-through. In the design, $L3$ and $L4$ are set to 5 μm and 1.5 μm respectively, and p++ interconnects are set at 8.5 μm apart with a tilt angle from centerline to enlarge the tight space. The isolation width between p++ interconnects and between the piezoresistor and the p++ interconnect are calculated to ensure that there is sufficient space to avoid punch-through considering space charge diffusion and lateral diffusion to the n-well. For the worst case, $V_j = -10V$ at left and 0V on the right, as shown in Figure 3-14, there is about 5 μm between p++ interconnects assuming a lateral diffusion of $\sim 1.3 \mu m$. At the edge of tethers, the p++ interconnects twist with a $\sim 60^\circ$ angle from the centerline of the tether to avoid bond pads implant punch-through.

In addition, attention needs to be paid to the piezoresistor and p++ interconnects to avoid crossover. As shown in Figure 3-15, the space charge layer between the piezoresistor and the n-well increase as depth increases. If the space between the piezoresistor and the p++ interconnect are too close, there will be crossover and the P region will punch through. A top view of the isolation width is shown in Figure 3-16, which is plotted in AutoCAD® 2002. The cyan region is the tether, the pink region is the p++ interconnects, the green region is the piezoresistor, and the blue line is the final isolation width considering lateral diffusion and space charge diffusion to the n-well.

In order to minimize the space charge diffusion to the n-well, one method is to increase the doping concentration of the n-well N_D . However, the internal electric field increases and the reverse junction breakdown voltage decreases as the n-well doping concentration increases. The breakdown voltage decreases from $\sim 50V$ to $\sim 10V$ when the impurity concentration increases from $1.0 \times 10^{16} \text{ cm}^{-3}$ to $1.0 \times 10^{17} \text{ cm}^{-3}$.

A sharp corner dramatically increases the stress concentration, which can lead to the failure of the materials. On the other hand, a sharp corner may increase the local electric field and decrease the breakdown voltage. In order to reduce the stress concentration, a sharp corner needs to be rounded, where the stress concentration factor depends on

¹⁰ Law, M.E. and S. Cea, *Continuum Based Modeling of Silicon Integrated Circuit Processing: An Object Oriented Approach*. Computational Materials Science, 1998. 12(1): p. 289-308.

the fillet radius for a given thickness. The concentration factor K is relatively high for the ratio of the fillet radius over a tether width of less than 0.5. In this design, K is chosen as 0.9 to reduce the stress concentration.

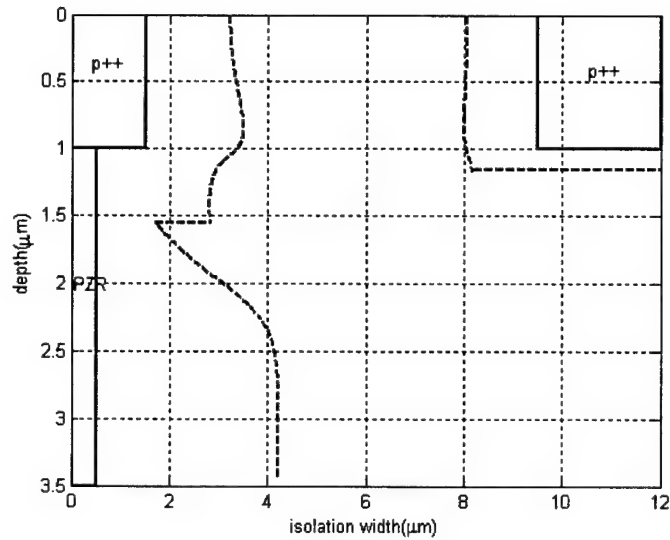


Figure 3-14 Cross-sectional view of isolation width between p^{++} interconnects.

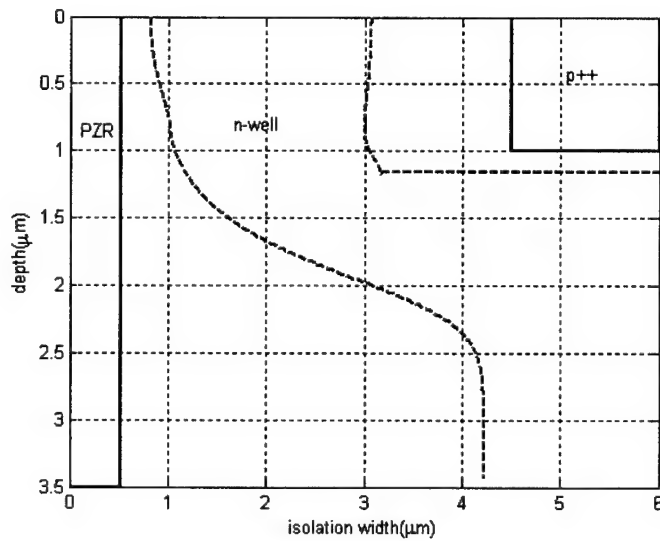


Figure 3-15 Cross view of isolation width between p^{++} interconnect and piezoresistor.

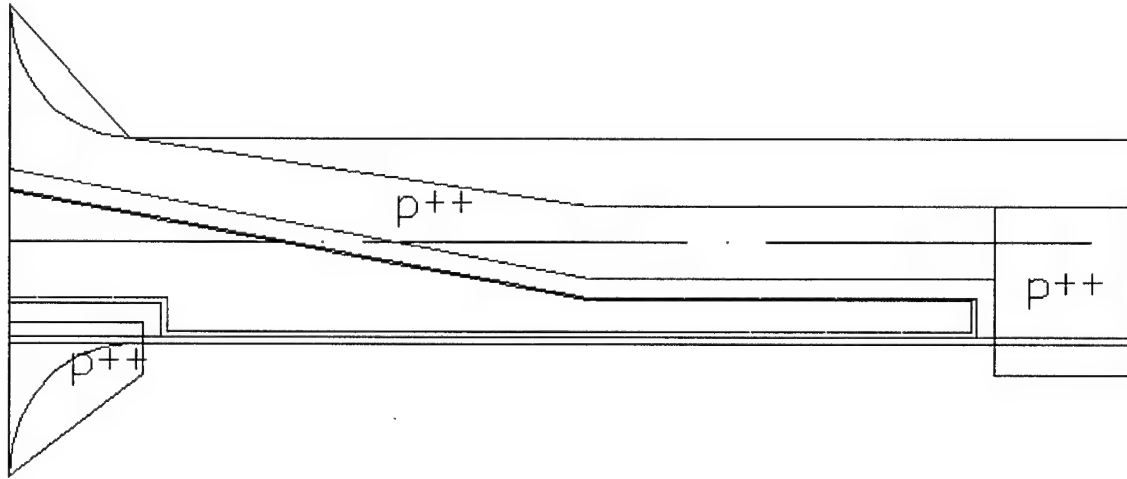


Figure 3-16: Top view drawing of the isolation width.

4 Optical Geometric Moiré-Interferometry-Based Piezoresistive Floating Element Shear Stress Sensor

In addition to the piezoresistive sensor, we are developing an optical-based sensor. Optical transducers possess several advantages in terms of immunity to electromagnetic interference and the potential of operating in higher temperature environments. For this project, we modified an existing, partially fabricated sensor design.¹¹ Therefore, only a few minor microfabrication steps were required to adapt the sensor to this application. In addition, these devices were not optimally designed for this application. The fabrication process flow for this sensor is less complicated than the piezoresistive sensor, but the sensor package was crude and constructed for preliminary bench-top characterization. The transition from bench-top proof of concept device to useful scientific instrument is nontrivial and will be one focus of the Phase II effort. During the past nine months, we have developed a comprehensive nonlinear electromechanical model of the sensor. In parallel with these efforts, a microfabrication process flow for the sensor was synthesized. Once the sensor design and process flow tasks were completed, a microfabrication mask set was generated and microfabrication completed. Bench top characterization of this device using a simple package was completed and testing in a simulated hypersonic environment conducted.

For the Moiré optical sensor, the displacement transducer consists of optical gratings on the backside of a floating element and on the top surface of the support wafer that superimpose light to form a Moiré fringe that amplifies the element translation as shown in Figure 4-1. The Moiré fringe pitch, G , is related to the individual grating pitches, g_1 and g_2 by

$$\frac{1}{g_1} - \frac{1}{g_2} = \frac{1}{G} \quad (37)$$

The Moiré fringe shift amplifies small displacements by the ratio of the fringe pitch, G , to the movable grating pitch, g_2 , and is invariant to intensity modulations.²¹ The displacement Δ of the Moiré fringe is

¹¹ Horowitz, S., Chen, T., Chandrasekaran, V., Tedjojuwono, K., Nishida, T., Cattafesta, L., and Sheplak, M., "A Wafer-Bonded, Floating Element Shear-Stress Sensor Using a Geometric Moiré Optical Transduction Technique," Technical Digest, Solid-State Sensor and Actuator Workshop, June 6-10, Hilton Head, SC, pp. 13-18, June 2004.

$$\Delta = \delta \left(\frac{G}{g_2} \right) \quad (38)$$

where δ is the physical displacement of the floating element displacement given by Equation (2). The Moiré fringe displacement is therefore amplified over the grating displacement by a factor of G/g_2 . For the device investigated in this study, $g_1 = 19 \mu m$, $g_2 = 10 \mu m$, and $G = 21 \mu m$.

The static and dynamic mechanical models describing this sensor are identical to those presented in Sections 3.1.1 and 3.1.2.

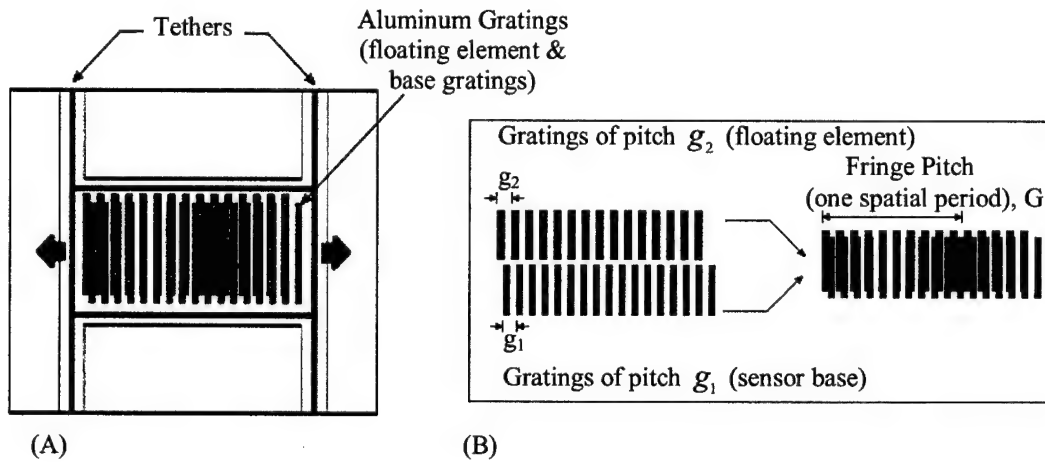


Figure 4-1: Conceptual top view schematic of the proposed optical shear-stress sensor (A) and associated Geometric Moiré pattern generated from two gratings (B)

4.1 Moiré Sensor Fabrication

The sensor was fabricated using an aligned wafer-bond/thin-back process that produces optical gratings on the backside of a floating element and on the top surface of the support wafer. The process flow consists of a 4-mask microfabrication process containing 8 major steps. The details of the wafer-bond/thin-back process are given in APPENDIX B. The photo-masks have been designed using AutoCAD® and have been fabricated. The microfabrication process has been completed. A optical photograph with a scanning electron microphotograph inset of the tether area is shown in Figure 4-2.

4.2 Moiré Sensor Testing

Prior to testing the sensor in the simulated hypersonic experiment, the sensor calibrated in a 2-D turbulent channel flow. The sensor was packaged by inserting the die flush-mounted in a Lucite plug with front-side imaging optics and a Thomson-CSF TH78CE13 linescan CCD camera. The CCD camera contains an array of 1×1024 pixels, each $10 \mu m$ in width capable of sampling at 37.8 kHz . The packaged device was then mounted into a $100 \text{ mm} \times 1 \text{ mm}$ flow cell that provides a variable mean shear stress (Figure 4-3) via a laminar and turbulent fully developed, 2-D pressure driven flow in a slot. The differential pressure between two locations in the fully-developed region of the flow cell is measured via a Heise pressure sensor, which is then used to compute the applied shear stress to the sensor. This differential pressure measurement is averaged 100 times and used to compute the applied shear stress τ_w via

$$\tau_w = -\frac{h \Delta p}{2 L}, \quad (39)$$

where Δp is the differential pressure, h is the height of the channel, and L is the distance separating the pressure ports.

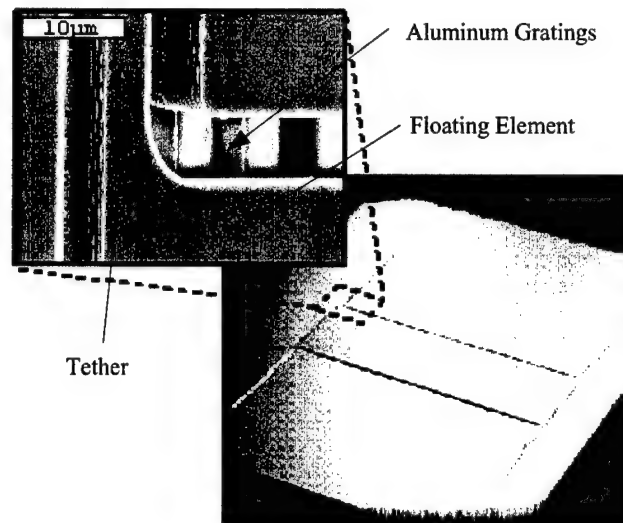


Figure 4-2: Top-view of the shear stress sensor using an optical profilometer. Inset: Close-up of tether and aluminum gratings taken using scanning-electron microscope (SEM).

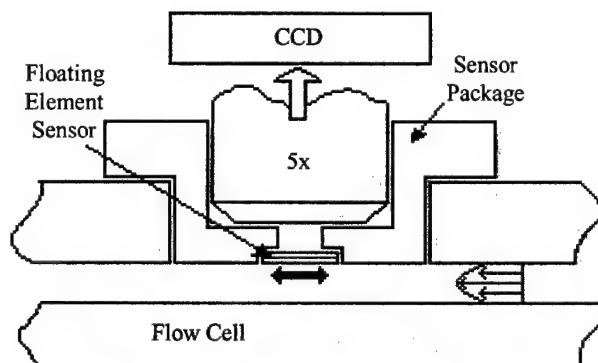


Figure 4-3: Schematic diagram of static calibration experimental setup illustrating backside imaging optics for 2-D laminar flow cell.

The Moiré fringe pattern is captured using the CCD camera, through the backside imaging optics. For the static calibration, 600 successive frames are obtained for averaging purposes. The imaged fringe pattern for zero applied shear stress is shown in Figure 4-4, where the first 100 successive frames from the camera are stacked vertically. The peak in relative intensity corresponds to the brightest region in the grayscale image.

From the captured image, relative pixel intensities are obtained for each frame and averaged over the 600 frames. The averaged relative pixel intensities obtained for two different shear stresses are shown in Figure 4-5. The resulting averaged intensity pattern is normalized by a calibration image to eliminate pixel gain variations and non-uniform illumination effects. Following this, a spatial Fast-Fourier Transform (FFT) is performed on the normalized fringe pattern, from which the phase of the Moiré pattern is then extracted. This phase is then compared against the phase calculated for zero applied shear stress to obtain the phase shift and the corresponding pixel shift. Using knowledge of the Moiré pattern and optical magnification, the corresponding mechanical displacement of the floating element is computed to give a direct measurement of the wall shear stress.

Following the procedure outlined above, the pixel shift of the Moiré fringe pattern was determined for a range of applied shear-stress. Representative laminar calibration results are shown in Figure 4-6, along with the

corresponding mechanical displacement for a $\tau_{\max} = 5 \text{ Pa}$ design. The mechanical sensitivity, as found from the slope of this curve, is $0.26 \text{ } \mu\text{m}/\text{Pa}$, while the Moiré fringe, after the 5x optical amplification, moves by $130.02 \text{ } \mu\text{m}/\text{Pa}$. Figure 4-6 illustrates a linear response up to 1.3 Pa .



Figure 4-4: Moiré fringe pattern for a static shear stress of 0 Pa as seen by 1024 pixel linescan camera. Successive frames from the camera are stacked vertically.

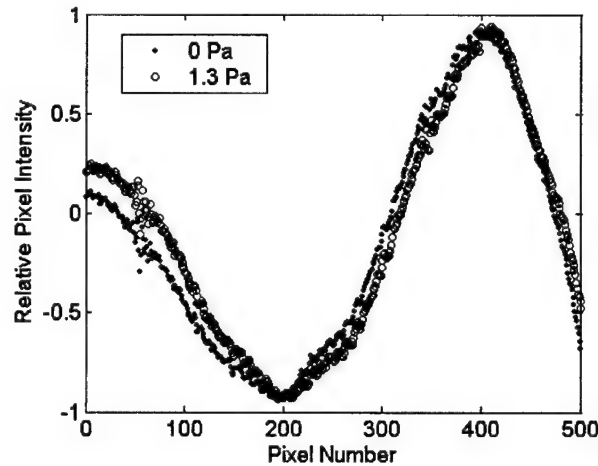


Figure 4-5: Measured relative pixel intensity for mean shear stresses of 0 Pa and 1.3 Pa .

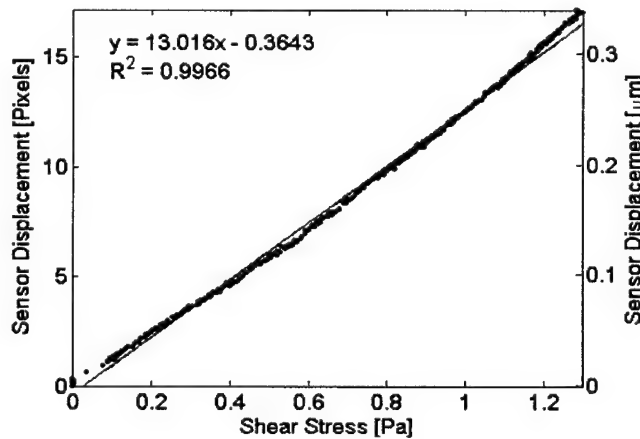


Figure 4-6: Representative static response of a $\tau_{\max} = 5 \text{ Pa}$ sensor in terms of Moiré fringe pixel displacement and corresponding mechanical displacement as a function of mean shear stress. The static sensitivities are $13.0 \text{ pixels}/\text{Pa}$ and $0.26 \text{ } \mu\text{m}/\text{Pa}$.

Representative turbulent channel flow calibration results are shown for a higher dynamic range sensor ($\tau_{\max} = 50 \text{ Pa}$) in Figure 4-7. The static sensitivity, as found from the slope of this curve, is $4.5 \text{ pixels}/\text{Pa}$. The lower sensitivity is expected for a stiffer device that was designed to maintain linearity up to 50 Pa . Time series data of the sensor was also taken in the turbulent channel flow in Figure 4-8 illustrated the ability to obtain time-resolved data.

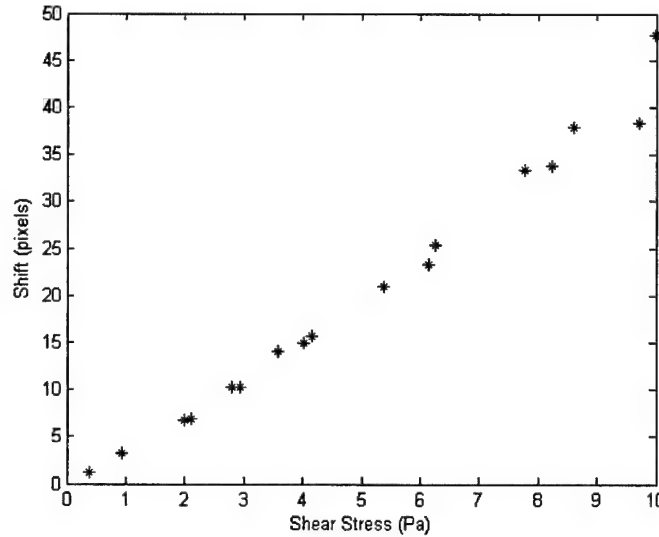


Figure 4-7: Representative static response of a $\tau_{\max} = 50 \text{ Pa}$ sensor in terms of Moiré fringe pixel displacement as a function of mean shear stress. The static sensitivity is 4.5 pixels/Pa.

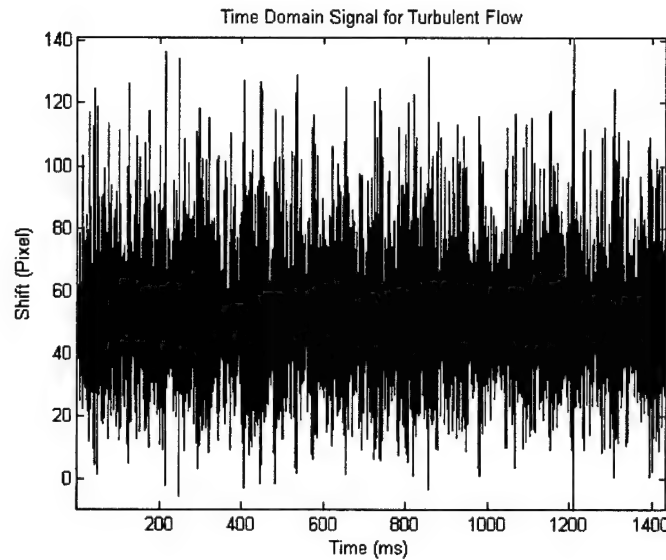


Figure 4-8: Representative time series data from a $\tau_{\max} = 50 \text{ Pa}$ sensor in terms of Moiré fringe pixel displacement in a turbulent channel flow possessing a mean shear stress of 10 Pa.

The recessed gap under the floating element gives rise to pressure-gradient induced errors. The magnitude of the effective shear-stress, τ_{eff} , acting in the presence of a pressure gradient has been shown to be

$$\tau_{\text{eff}} = \left(1 + \frac{g}{h} + \frac{2t}{h} \right) \tau_w, \quad (40)$$

where h is the channel height of the wind tunnel used for calibration and g is the recessed gap. The second and third terms in the bracket are the error terms associated with flow under the floating element and the pressure gradient acting on the lip of the element, respectively. For the current device and experimental apparatus, this component of the calibration error is 2%.

After bench-top characterization of complete in the flow cell, a new sensor package was designed to facilitate testing in the supersonic tunnel. A schematic of the packaged device inserted into the supersonic wind tunnel is shown Figure 4-9. The finished device was then packaged by flush-mounting the sensor die in a Lucite plug with back-side imaging optics, providing a 5x optical magnification, and a Thomson-CSF TH78CE13 linescan CCD camera attached to the end of a 12 inch rigid Hawkeye Slim borescope. A Labview workstation controls the flow through the wind tunnel and the Moiré patterns are acquired using a frame grabber on a different computer.

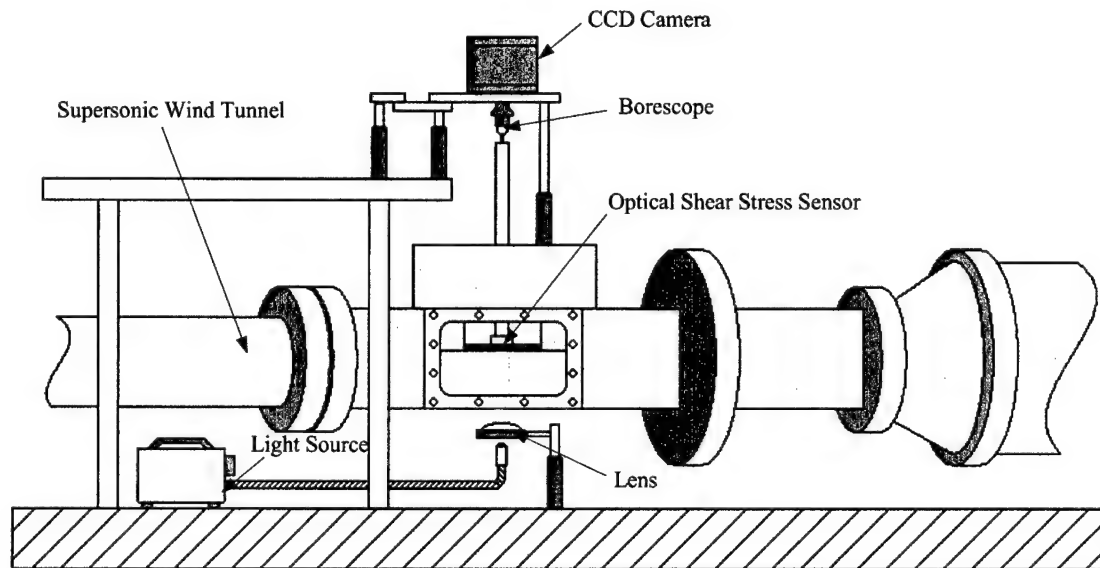


Figure 4-9: A schematic representation of the optical shear stress sensor setup for the supersonic wind tunnel.

The device was tested up in a nozzle wall turbulent boundary layer to $\tau_{\max} \approx 320 \text{ Pa}$ at $M = 1.6$. The floating element sensor survived multiple runs, but the borescope-based imaging system proved to provide inadequate resolution to accurately capture the fringe shifts. While we feel that this technique is very promising, clearly improvements must be made in the optical package to permit wind-tunnel measurements.

5 Test Facility Development and Characterization

In preparation for testing the MEMS shear stress sensors, conventional shear stress measurements using laser skin friction interferometry for calibration purposes were performed a prototypical high-speed flow in the Fluid Mechanics Laboratory at the University of Florida.

5.1 Interferometric Skin Friction Measurements

An interferometric skin friction instrument and corresponding software was created to obtain skin friction measurements on a polished stainless-steel plate in supersonic flow. The instrument followed that of global interferometric skin friction (GISF) system¹² which uses full-field images to directly compute the oil-film slope with respect to time. The measurements were acquired to provide a means to calibrate the MEMS-based optical shear stress sensor. The chosen flow environment was a small-scale, supersonic, blow-down test stand. The test stand stagnation chamber was supplied with high-pressure air from an in-house compressor (200 psi, 1000 scfm) by means of a 1.5" \varnothing pneumatic control valve. A nozzle block (4 in² cross-sectional area) was connected to the stagnation

¹² Naughton, J. W., and Sheplak, M., "Modern Developments in Shear Stress Measurements," *Progress in Aerospace Sciences*, 2003

chamber. The freestream Mach number just upstream of the cavity is 1.45^{13} . Aft of the nozzle block (approximately 18" from the throat) was an adjustable depth cavity. The cavity block created a steady (zero depth) or unsteady flow environment. The oil-film measurements were conducted in the steady flow environment. The floor of the cavity block was a polished stainless steel plate suitable for optical-based skin friction measurements. The stagnation test conditions were computer controlled and flow parameters (stagnation and static pressures, stagnation and wall temperatures) are monitored using a LabVIEW virtual instrument

An image and corresponding schematic of the GISF instrumentation is shown in Figure 5-1 and Figure 5-2. The excitation from a UV lamp was directed toward the cavity floor. The lamp excitation was attenuated and diffused using two diffusion glass plates. The light then passed through a beam splitter plate prior to impinging the cavity floor. The reflected light off the polished floor was turned 90 degrees by the beam splitter toward a CCD camera. Fitted to the camera was a 300 mm zoom lens. The corresponding linear pixel density for the oil film tests was $81 \mu\text{m}/\text{pixel}$. The reflected excitation from the oil film was filtered with a 450 nm broadband interference filter to capture the 436 nm triplet lines of the mercury vapor lamp and reject other excitation wavelengths. All GISF tests were conducted with the polished plate aligned with the nozzle floor (no cavity depth, steady flow conditions).

Prior to the skin friction tests, the GISF instrumentation was aligned, focused, and calibrated (determination of the linear pixel density). Images were acquired using a Photometrics Series 300 CCD camera (a slow scan, 16-bit imager, 512×512 imager). The camera was controlled by a second PC. A LabVIEW program was used to capture camera images as well as a synchronization voltage from the test stand PC. Dow silicon Series 200 oils were used in the experiments. The oil viscosity was measured prior to the tunnel runs using a Wells-Brookfield cone-plate digital viscometer. Results of the calibration tests for four viscosities are shown in Table 5-1.

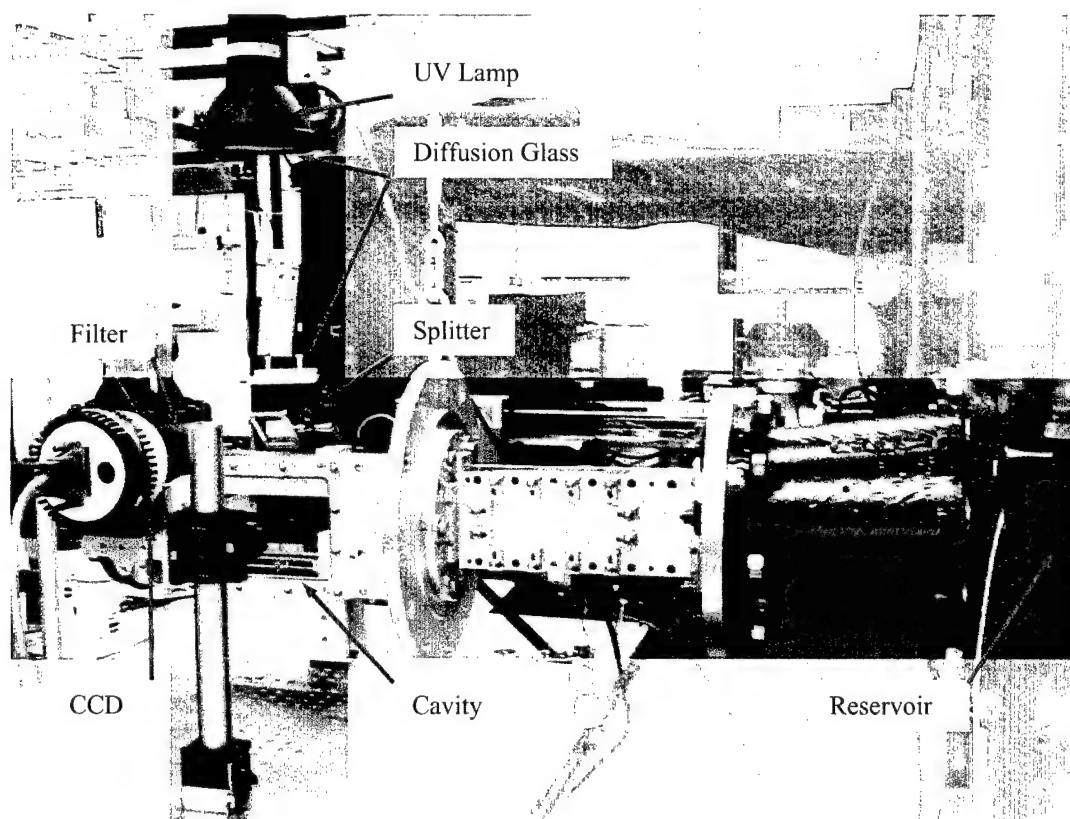


Figure 5-1: Image of the GISF instrumentation.

¹³ The freestream Mach number decreases along the length of the constant area nozzle block due boundary-layer growth. This is a mild function of stagnation pressure and distance from throat.

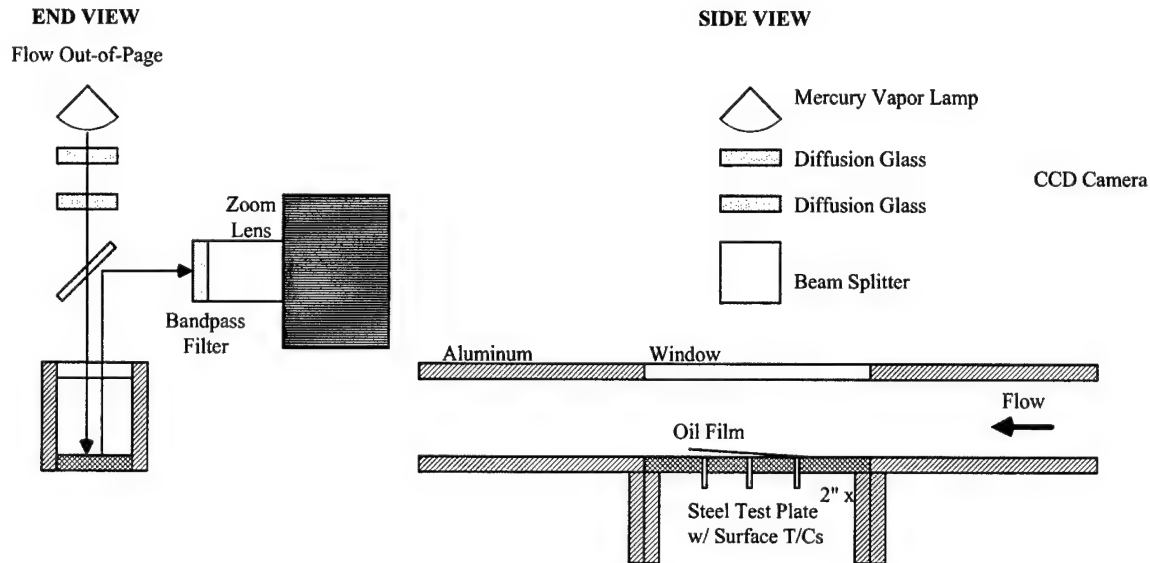


Figure 5-2: Schematic of the GISF instrumentation.

Table 5-1: Measured Oil Viscosity ($T_{ref} = 25\text{ }^{\circ}\text{C}$)

Oil	ν [cS] $\pm 5\%$
20	21
50	52
100	106
200	213

$\text{cS} = 1 \times 10^{-6} \text{ m}^2/\text{s}$

Of the four calibrated oils, the 200 cS oil was most suitable for the shear level along the polished plate at supersonic flow conditions. A small drop of the oil was placed on the center of the test plate. The sidewall was refastened, and the tunnel was started. Within approximately 5 s, the test section stagnation pressure level was achieved. Because a constant supply voltage was maintained, the pressure slowly dropped during the run (Figure 5-3). Averaged flow conditions during the image acquisition were used in the shear calculations. Images (exposure time = 500 ms) were acquired at intervals of approximately 5 to 10 s (Figure 5-4).

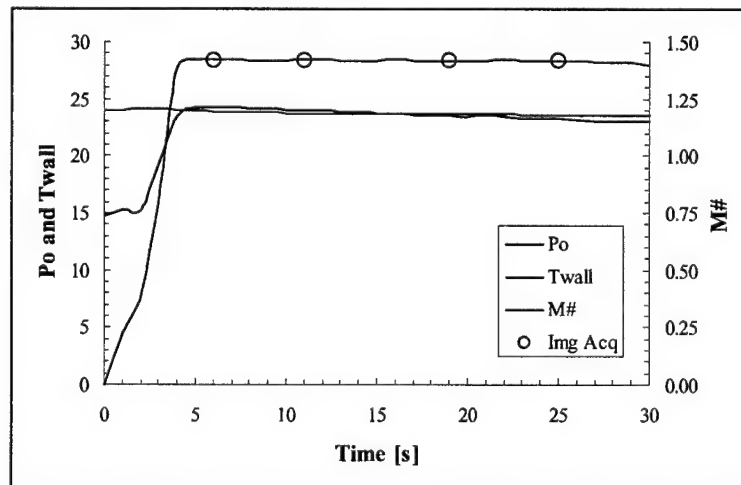


Figure 5-3: Tunnel conditions during a typical run (Test G).

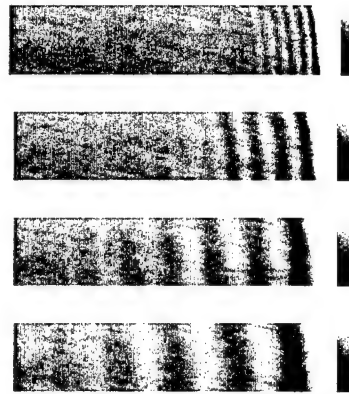


Figure 5-4: Sample fringe images during tunnel run: flow right to left

The fringe images were viewed using Image Viewer.vi. The intensity of ten rows (0.8 mm) were averaged and saved in a text file. This file was read and analyzed by Fringe Spacing.vi to determine the oil film slope using a correlation routine and assuming linear deformation over the area analyzed. Finally, GISF Shear Calculator.vi was used to calculate the acting shear stress over the first four fringe images. The calculation of the skin friction coefficient, C_f , was determined using

$$C_f = \frac{\tau}{q_\infty} = \frac{\frac{2n}{\lambda} \cos(\theta_r) \Delta x}{\int_{t_0}^{t_1} \frac{q_\infty}{\mu} dt}, \quad (41)$$

where q_∞ is the dynamic pressure, n is the oil index of refraction, λ is the light wavelength, θ_r is the oil light refraction angle, Δx is the spatial fringe spacing between times t_1 and t_0 , μ is the oil absolute viscosity, and t is the time. The calculation assumes the oil temperature is that of the wall temperature. The average wall temperature and dynamic pressure during the run interval is used in the calculation. Results from nine test runs at various stagnation pressure levels are shown in Table 5-2. As expected, increasing the tunnel stagnation pressure and hence dynamic pressure increases the acting shear stress level. At the highest tested stagnation level, 51 psia, the wall shear stress and coefficient were 310 Pa and 0.00205, respectively. Note that at pressure levels below 22 psia, the tunnel becomes unchoked, the flow is subsonic, and the shear stress coefficient increases due to the higher relative drop in the dynamic pressure compared to the acting shear stress. Overall measurement uncertainty is 6-8% primarily due to the uncertainty in the oil viscosity.

Table 5-2: Shear stress results along the polished cavity plate (zero depth)

Test	Po [Pa]	To [C]	M	q [kPa]	τ [Pa]	Cf	Re/l
A	50.9	24.8	1.46	151.0	313	0.00207	5.20E+07
B	51.1	25.2	1.46	151.8	310	0.00205	5.22E+07
C	48.0	25.3	1.45	142.6	293	0.00205	4.90E+07
D	45.6	25.8	1.46	135.4	289	0.00213	4.65E+07
E	40.0	25.9	1.45	118.8	252	0.00212	4.07E+07
F	28.5	25.8	1.44	84.7	172	0.00203	2.92E+07
G	23.7	26.2	1.42	70.5	133	0.00189	2.43E+07
H	16.7	26.2	0.53	18.8	64	0.00342	1.19E+07
I	15.4	25.0	0.31	6.6	26	0.00396	6.96E+06

6 Conclusions

- 1) We have developed and verified detailed, novel electromechanical models of for a silicon micromachined piezoresistive floating element shear-stress sensor possessing through-wafer backside electrical contacts for unsteady hypersonic flow measurement applications. These models have been used to optimally design 6 devices for various target flow applications. A process flow has been developed and is over 50% complete with roughly 3 weeks remaining until completion. Phase II work will include transitioning this microfabrication process to a commercial fabrication facility to improve quality and reduce turn around time. In addition, the device packaging will also be contracted out to a professional packaging house. We have visited both microfabrication foundries and packaging vendors and waiting for quotations regarding the complete manufacturing and packaging of these devices.
- 2) We have also developed a floating-element shear-stress sensor employing an optical Moiré transduction technique. While this device represented a proof of concept of the transduction technique, it possessed the following limitations that we will address during Phase II:
 - The device modeling was preliminary resulting in poor agreement between theory and experiment. In addition, device optimization was not performed. Rigorous optical and mechanical modeling is needed for optimal design purposes.
 - The sensor package was crude and constructed for preliminary bench-top characterization underneath a microscope. The transition from bench-top proof of concept device to useful scientific instrument needs to be the main focus of additional efforts. Specifically, we are investigating teaming with Viosense Corporation to develop a micro-optical integrated imaging system that will greatly improve the packaging of this device.
 - The microfabrication and packaging of this device also needs to be contracted out to commercial foundries to ensure high quality, reliable operation.
- 3) While both devices possess back side transduction read-outs, there are additional robustness issues concerning the physical protection of the floating element and the thermal isolation of the sensor that need to be addressed in Phase II. One drawback to floating element sensors is the inherent gaps present to permit the sensing element to translate under the action of an applied shear stress. These gaps have the potential to become clogged with debris, thus altering the sensor response. While the inherently small gap size $O(1\mu m)$ of the proposed device will greatly reduce pressure gradient errors and flow perturbations, it will also spatially filter the particle size that can be trapped in the recessed gaps. Regardless, several techniques will be evaluated to solve this issue. Specifically, we will investigate effect of filling the gap with oil and/or compliant polymer to provide a physical barrier to debris. We will determine the impact on the static and dynamic device response via finite-element simulations. We will also investigate the application of a thin polymer coating (such as Parylene) over the top surface of the sensor to protect the sensor gaps from debris. The effects of these coatings on the sensitivity, linearity, and frequency response will be quantified both computationally and experimentally. An additional potential benefit of using a Parylene coating is that it is a low thermal-conductivity material that will provide some degree of a thermal barrier for moderate enthalpy flows.

7 Equipment Acquisition

No equipment was acquired as part of this contract.

8 APPENDIX A

8.1 Fabrication Process Flow for Piezoresistive-Based Floating Element Sensor

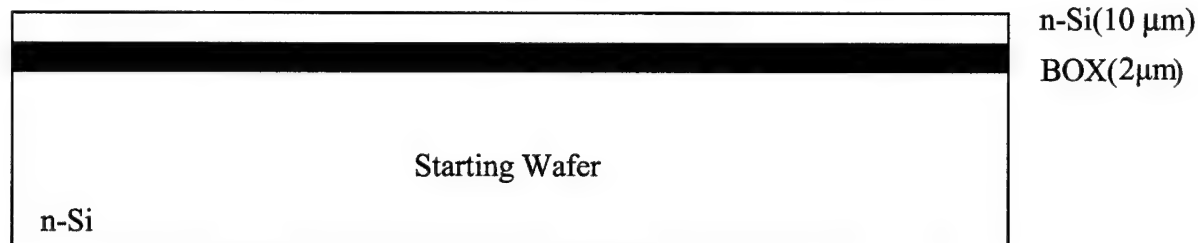
**SIDE-IMPLANTED PIEZORESISTIVE SHEAR STRESS
SENSOR
WITH INTEGRATED ELECTRICAL THROUGH-WAFER INTERCONNECTS**

Lot: Shear Stress_UF_1.1

Lot Owner : Interdisciplinary Microsystem Group, Gainesville, FL

Wafer: 4" n-type (100) SOI wafer, Resistivity: 1~5 ohm-cm

Step	Step No	Lab/Equip	Process Description
Starting Wafer	0	TRL	Start with SOI wafer with 10 um silicon on 2 um BOX



Pattern Through-wafer Vias	1.1	TRL/Wet Bench	Pre-oxidation RCA clean
	1.2	TRL/Tube B3	Grow 2 um of thermal oxide at 1100 °C
	1.3	TRL/Coater	Spin photoresist on front surface, 12 um (AZ9260) Prebake, 95 C, 30 min Spin photoresist on back surface, 12 um (AZ9260) Prebake, 95 C, 60 min
	1.4	TRL/EV1	Patterned both sides by Hole Mask (HM) Expose for 45 sec (15*10*3)

Develop, AZ440, 2 min 15 sec
Postbake, 95 C, 30 min

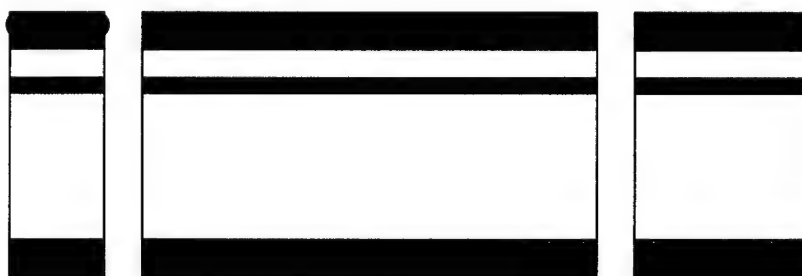
1.5 TRL/Wet Bench BOE
Piranha - 20 min



(1.2 - 1.5)

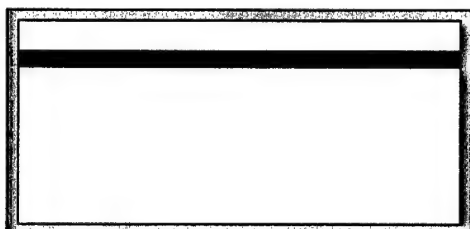
**Etch
Through-
wafer Vias**

- | | | |
|-----|---------------|--|
| 2.1 | TRL/STS2 | Etch alignment marks (and cover with tape)
Etch the front side up to the BOX |
| 2.2 | TRL/Wet Bench | Etch BOX, BOE |
| 2.3 | TRL/STS2 | Etch from back side (~210 min) (roughly half the wafer thickness)
Continue from front side - finish through-wafer vias (~210 min)
Timed overetch with support wafer (30 min) |
| 2.4 | TRL/Asher | Ash strip resist |
| 2.5 | TRL/Wet Bench | Pirahna |



**Oxide
Insulation**

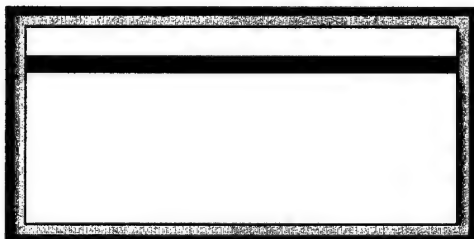
- | | | |
|-----|---------------|-----------------------------------|
| 3.1 | TRL/Wet Bench | Pre-oxidation RCA clean |
| 3.2 | TRL/Tube B3 | Grow 2 um thermal oxide at 1150 C |



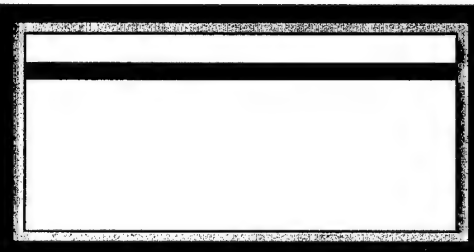
**Deposit/Dope
Polysilicon
Conduction
Layer**

- | | | |
|-----|---------------|---|
| 4.1 | TRL/Wet Bench | Pre-oxidation RCA clean |
| 4.2 | TRL/Poly Tube | Deposit 2 um polysilicon (165 min)
Inspect - make sure light passes through all holes

Dope polysilicon with boron |
| 4.3 | TRL/Tube B3 | Oxidize doped polysilicon at 1000 C |
| 4.4 | TRL/Wet Bench | Etch borosilicate glass, BOE (60 min) |
| 4.5 | TRL/Wet Bench | Pre-oxidation RCA clean
Repeat polysilicon deposition and doping |



(4.2 - 4.5)



**Fill TWV
holes**

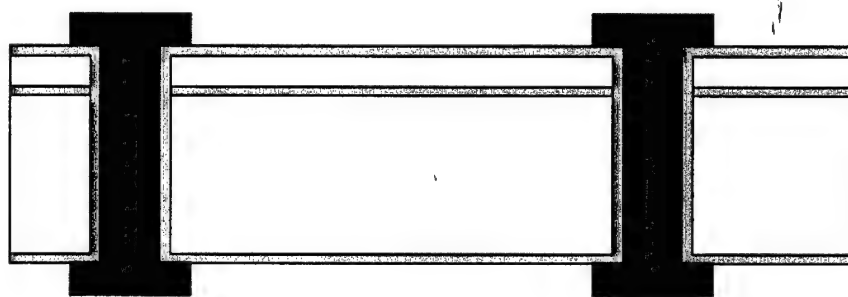
- | | | |
|-----|---------------|---------------------------------------|
| 5.1 | TRL/Poly Tube | Deposit 3 um of polysilicon |
| | | Dope surface polysilicon with boron |
| 5.2 | TRL/Tube B3 | Oxidize doped polysilicon at 1000 C |
| 5.3 | TRL/Wet Bench | Etch borosilicate glass, BOE (60 min) |
| 5.4 | TRL/Wet Bench | Pre-oxidation RCA clean |
| 5.5 | TRL/Tube B3 | Anneal at 1000 C for 1 hr |

(5.1 - 5.3)

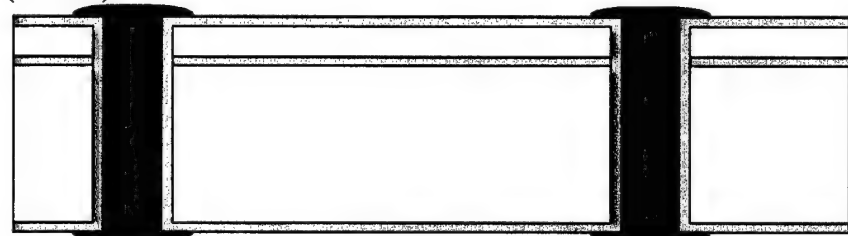


**Pattern
Polysilicon
Bond Pads**

- | | | |
|-----|---------------|--|
| 6.1 | TRL/Coater | Spin photoresist on front surface, 12 um (AZ9260)
Prebake, 95 C, 30 min |
| | | Spin photoresist on back surface, 12 um (AZ9260)
Prebake, 95 C, 60 min |
| 6.2 | TRL/EV1 | Patterned by SGM |
| | | Expose for 45 sec (15*10*3)
Develop, AZ440, 2 min 15 sec
Postbake, 95 C, 30 min |
| 6.3 | TRL/STS2 | Etch polysilicon on the front side
Etch polysilicon on the back side
Note: Repeat polysilicon etch in steps of 1-2 um to prevent wafer bow |
| 6.4 | TRL/Wet Bench | Pirahna |
| 6.5 | TRL/STS2 | Isotropic etch (to reduce step height of polysilicon bond pads) |

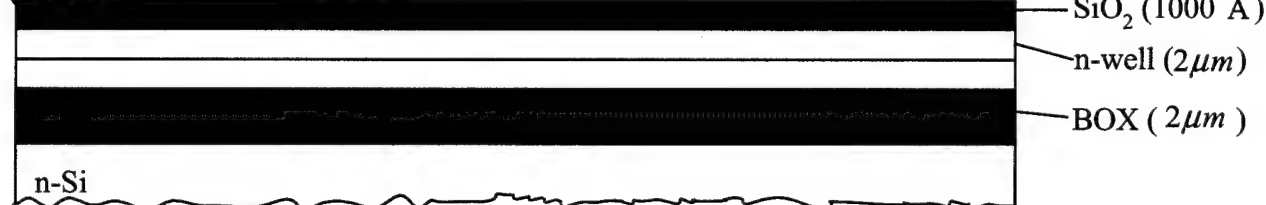


(6.1 - 6.5)

**n-well
Implant**

7.1	Core Systems, CA Implanter	Ion Implant: dopant = phosphorus, energy = 150 keV, dose = $6.0 \times 10^{12} / \text{cm}^2$ Blanket implant front surface.
7.2	TRL/Wet Bench	Pirahna (2x)
7.3	TRL/RCA	Pre-oxidation RCA clean
7.4	TRL/Tube B3	Grow 1000 Å dry oxide at 1050 C for 92 min

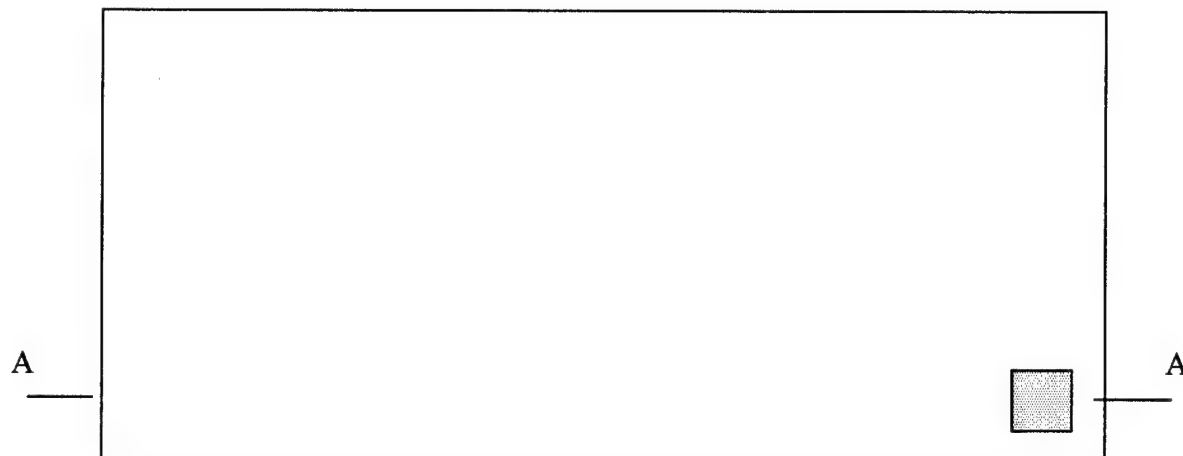
(7.1 - 7.4)

**Reverse Bias
Contact**

8.1	TRL/Coater	Spin photoresist on front surface, AZ9260, 12 μm Prebake, 95 C, 60 min
8.2	TRL/EV1	Patterned by Reverse Bias Mask (RBM) Expose for 45 sec (15*10*3) Develop, AZ440, 2 min 15 sec Postbake, 95 C, 30 min

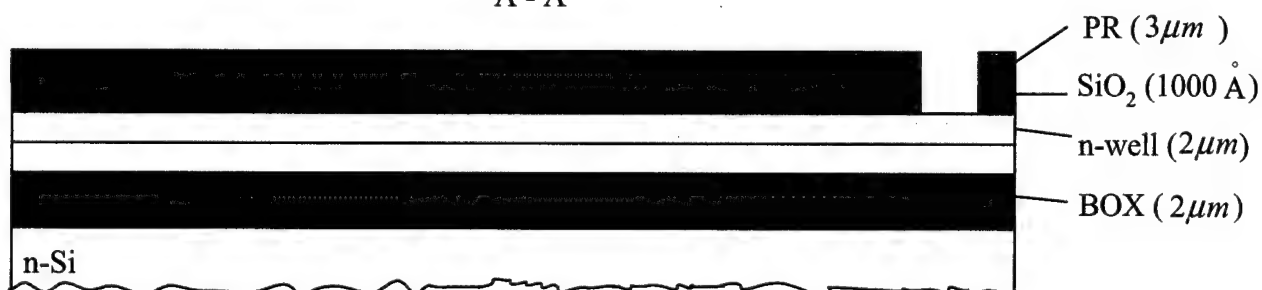
- 8.3 TRL/Wet Bench BOE etch, stop at silicon layer
this step puts the alignment marks on the oxide

(RBM)



A - A

(8.1 - 8.3)



- | | | |
|-----|----------------------------------|---|
| 8.4 | Core Systems,
CA
Implanter | Ion Implant: dopant =Arsenic, energy = 150 keV, dose = $6.0 \times 10^{15} / \text{cm}^2$ |
| 8.5 | TRL/Wet Bench | Strip photoresist, Pirahna (2x) |
| 8.6 | TRL/RCA | Pre-oxidation RCA clean |
| 8.7 | TRL/Tube B3 | Anneal at 1000 C for 420 min |

Implant

Piezo

"Contact"

9.1

TRL/Coater

Spin photoresist on front surface, AZ9260, 12 μm
Prebake, 95 C, 60 min

TRL/EV1

Pattern ohmic "contact" via **Piezo Contact Mask (PCM)**
Align to the marks created via **RBM**

Expose for 45 sec (15×10^3)
Develop, AZ440, 2 min 15 sec
Postbake, 95 C, 30 min

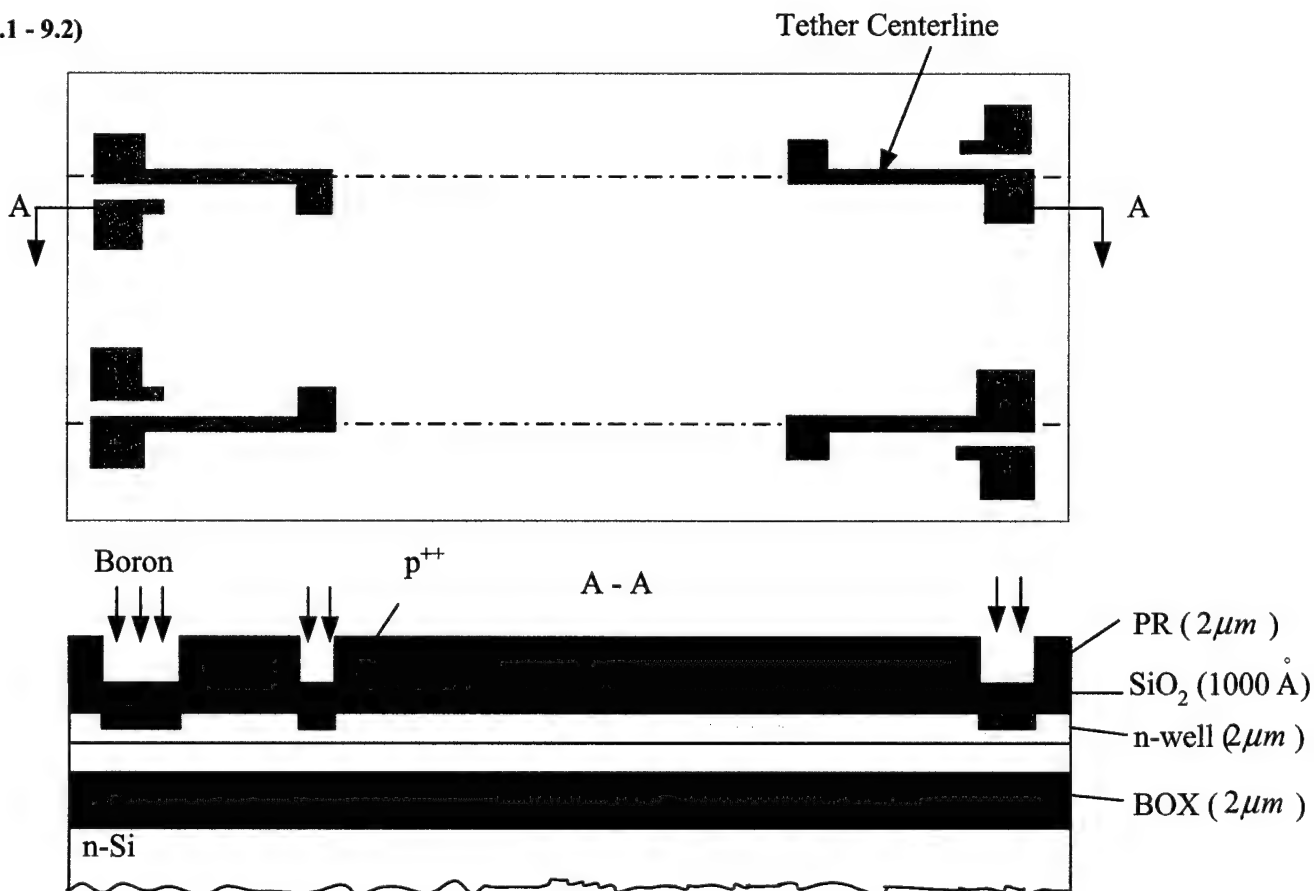
9.2

Core Systems,
CA
Implanter

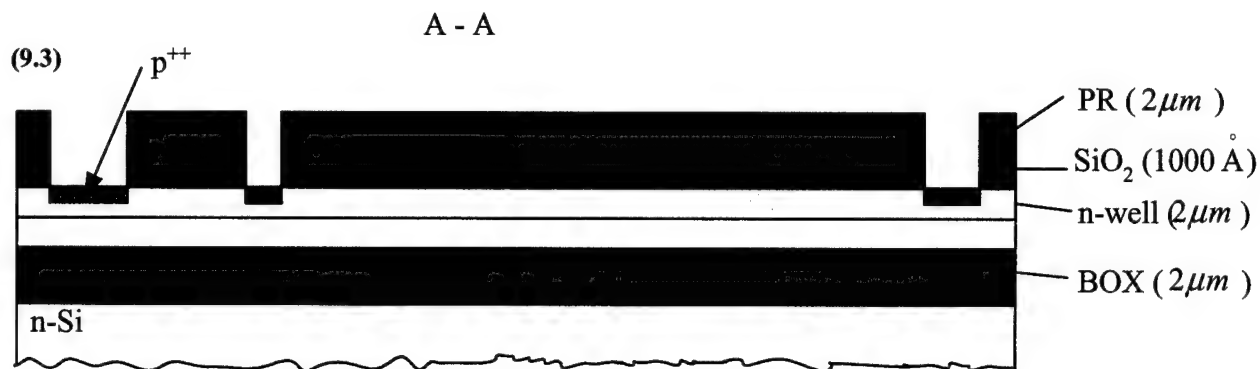
Ion Implant: dopant = boron, energy = 50 keV, dose = $6.2 \times 10^{15} / \text{cm}^2$

(PCM)

(9.1 - 9.2)



- 9.3 TRL/Wet Bench Etch oxide (BOE)
This step puts new alignment marks on the oxide



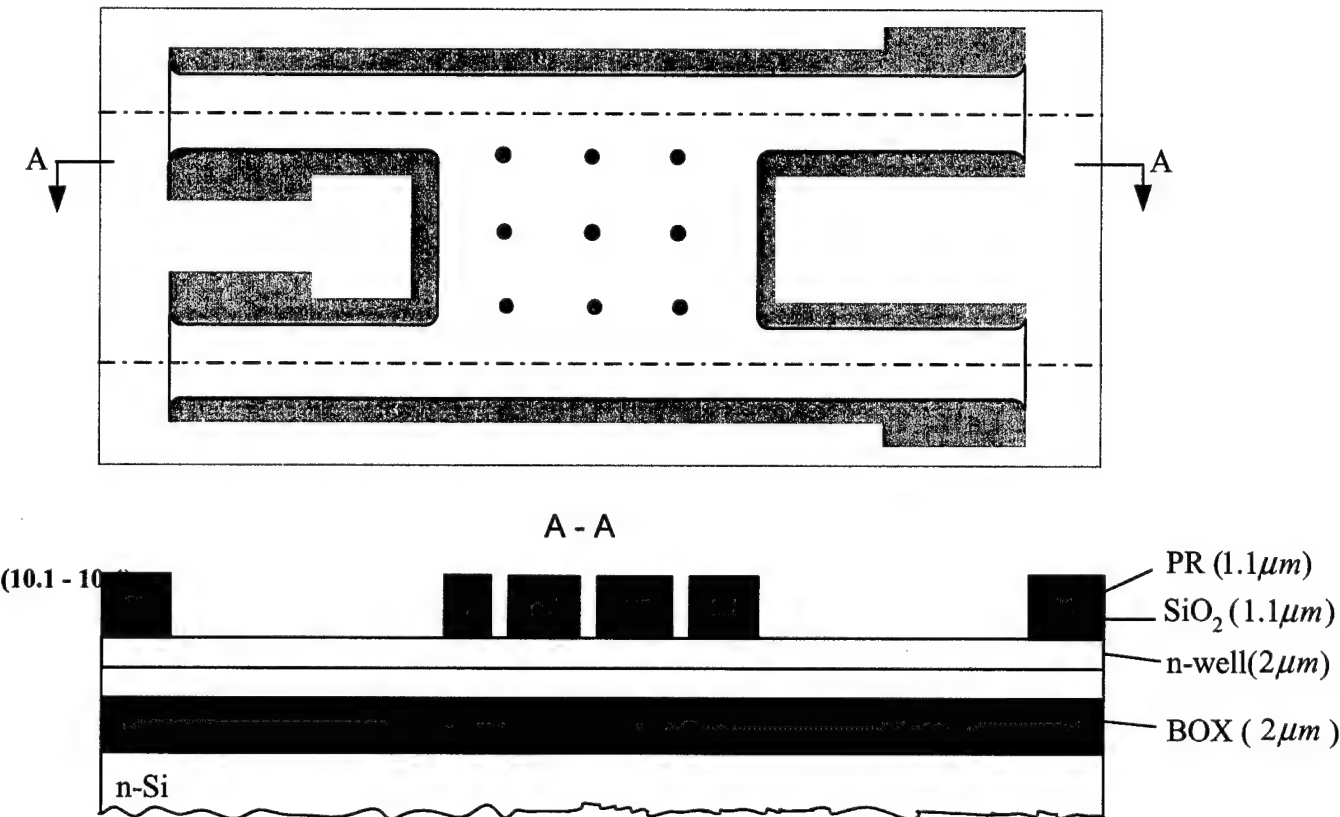
- 9.4 TRL/Asher Ash photoresist
- TRL/Wet bench Piranha clean (2x)
- 9.5 TRL/RCA Pre-oxidation RCA clean
- 9.6 TRL/Tube B3 Anneal at 1000 C for 120 min

Nested Mask Release

- 10.1 TRL/Tube 6 Deposit 1 um LPCVD Oxide
- 10.2 TRL/Coater Spin photoresist on front surface, OCG825, 0.5k/0.75k/2k, 6s/6s/30s, 1.1 um
Prebake, 95 C, 30 min
- 10.3 TRL/EV1 Pattern structure using **Nested Mask (NM)**
Align to the marks created via **PCM**
- Expose for 2 secs
Develop, OCG934, 1 min
Postbake, 95 C, 30 min

10.4 TRL/Wet Bench Etch oxide (BOE)
 This step puts new alignment marks on the oxide

(NM)



**Etch
Sidewalls**

- | | | |
|------|---------------|--|
| 10.5 | TRL/Asher | Strip photoresist |
| 10.6 | TRL/Wet Bench | Pirahna clean |
| 11.1 | TRL/Coater | Spin photoresist on front surface, AZ9260, 10 um
Prebake, 95 C, 60 min |
| 11.2 | TRL/EV1 | Pattern trench for side-wall implant using Side Implantation Mask (SIM)
Align to alignment marks created by NM.

Expose for 45 sec (15*10*3)
Develop, AZ440, 2 min 15 sec
Postbake, 95 C, 30 min |
| 11.3 | TRL/Wet Bench | BOE dip (~30 s)
Prior to DRIE to remove native oxide |

- 11.4

TRL/STS2

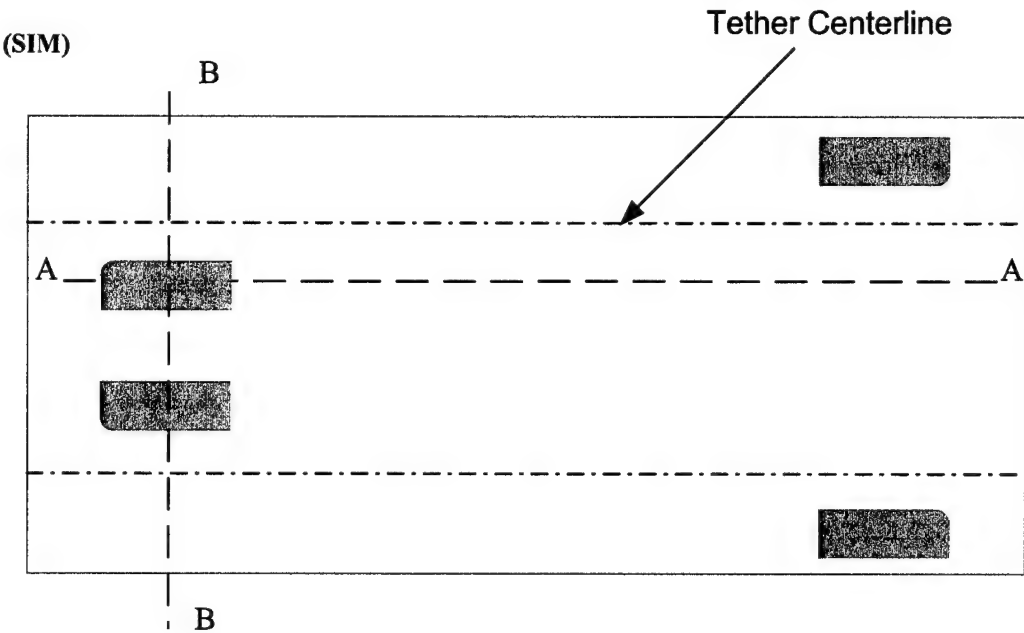
DRIE active silicon layer upto the BOX

O2 clean

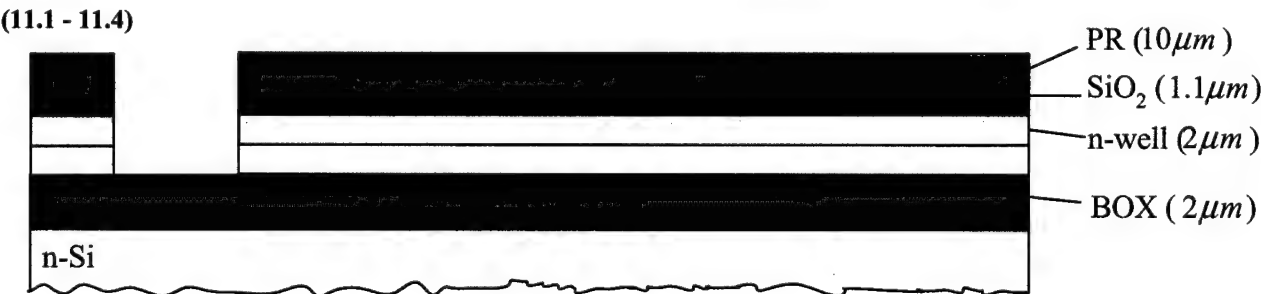
depth H=thickness of Si on top (10 um)

Length L=length of the piezoresistor + Overlap length (20 um)

width > tan31*(H + thickness of oxide + thickness of the photoresist)



A-A



- Side-wall
Implantation

12.1

Core systems, CA
Implanter

Ion implant: dopant=Si, energy=50 keV, dose=1e+15/cm^2, 31 deg tilt
preamorphization implant to minimize defect

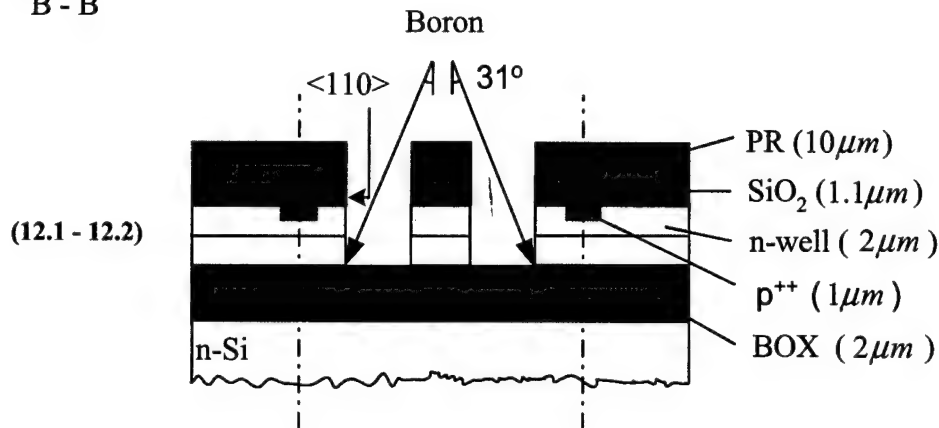
Make Si Rp > actual B implant Rp + 2*delta_RP
- 12.2

Core systems, CA
Implanter

Ion Implant: dopant = boron, energy = 10 keV, dose = 2.1e+14 /cm^2
31 deg tilt

- | | | |
|------|------------------------|--|
| 12.3 | TRL/Asher
Wet Bench | Strip photoresist
Pirahna clean (2x) |
| 12.4 | TRL/RTA | Rapid thermal annealing (RTA)
start.temp=700, ramp=100, cool=80, dwell.temp=1100, dwell.time=60 sec
Annealing temp=1000 C, time=23 min |

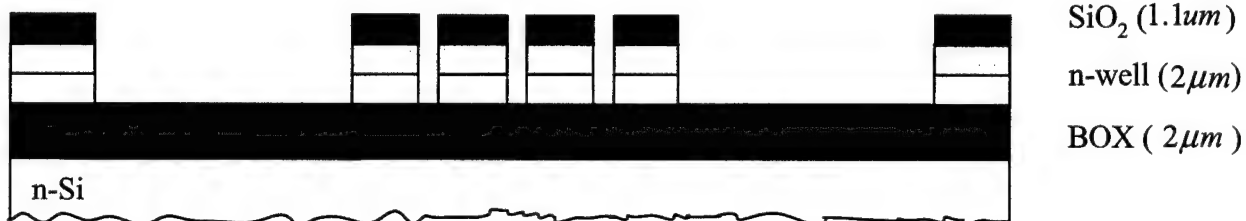
B - B



Partial
Release

- | | | |
|------|--------------------------|--|
| 13.1 | TRL/Wet Bench
piranha | pre-DRIE piranha clean
very short HF dip, don't remove more than 50 Å |
| 13.2 | TRL/STS2 | Plasma etch using nested mask upto BOX |

(13.2)



- | | | |
|------|----------------------|---|
| 13.3 | TRL/Coater
coater | Spin photoresist on front surface, AZ9260, 12 μm
Prebake, 95 C, 60 min |
| 13.4 | TRL/EV1 | Pattern tethers using Partial Release Mask (PRM)
Align to the marks created via NM

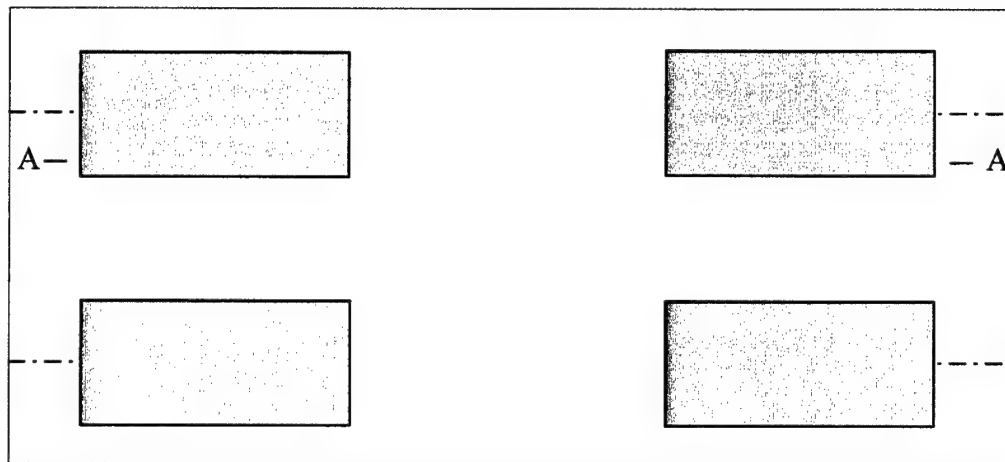
Expose for 45 sec (15*10*3)
Develop, AZ440, 2 min 15 sec
Postbake, 95 C, 30 min |

13.5 TRL/Wet Bench Etch oxide (BOE)

Release Only the tethers

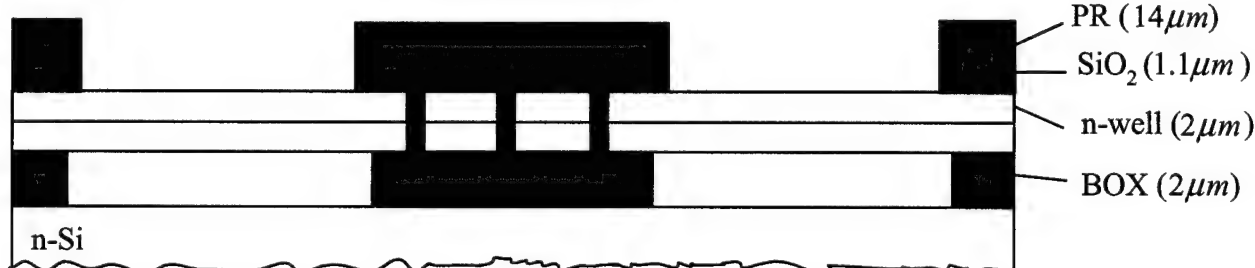
(PRM)

This step put new alignment marks



(13.3 - 13.5)

A - A

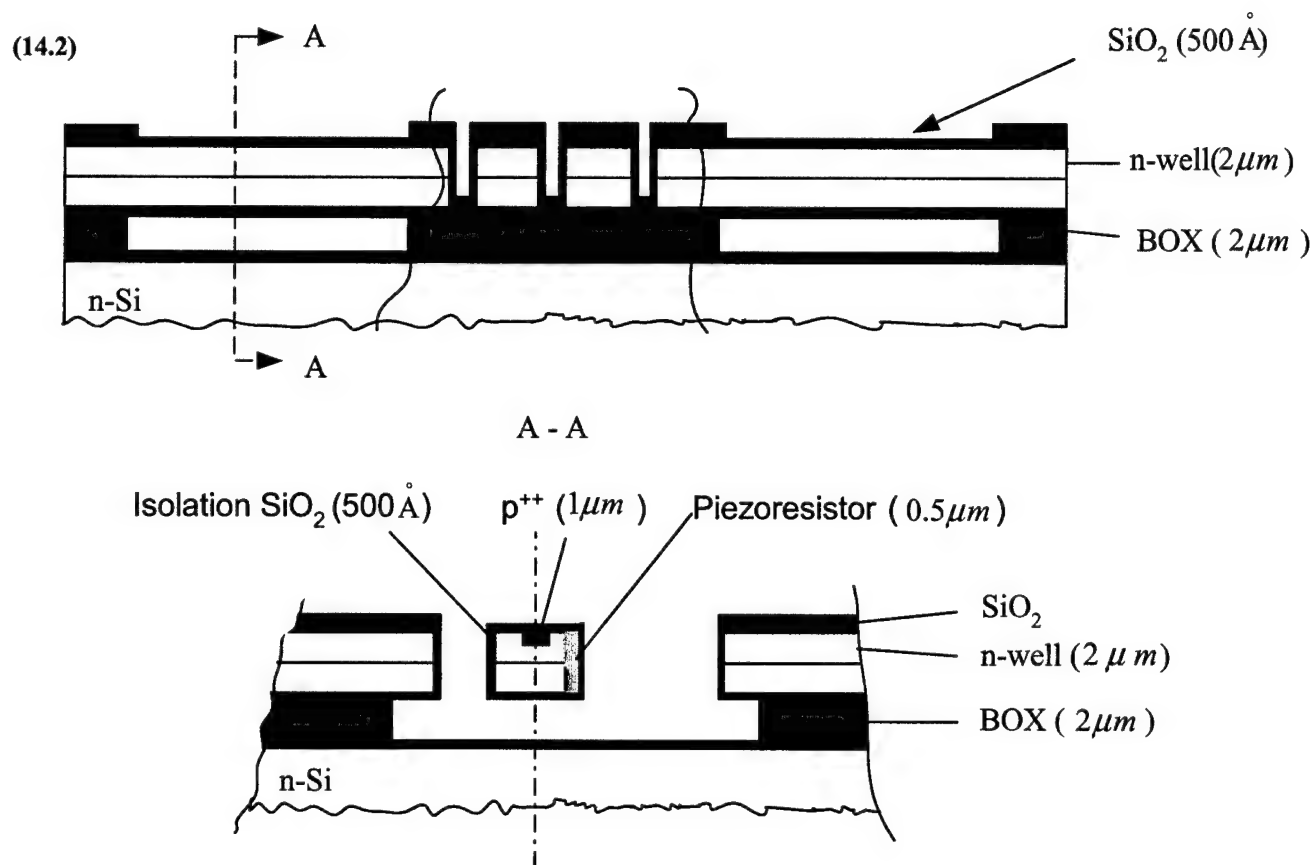


13.6 TRL/Asher Strip photoresist
TRL/Wet Bench Pirahna clean

Oxidation 14.1 TRL/RCA Station RCA clean
Preoxidation clean

14.2 TRL/TubeB2 Grow 500 Å dry oxide at 975 deg
Time=82.3 min

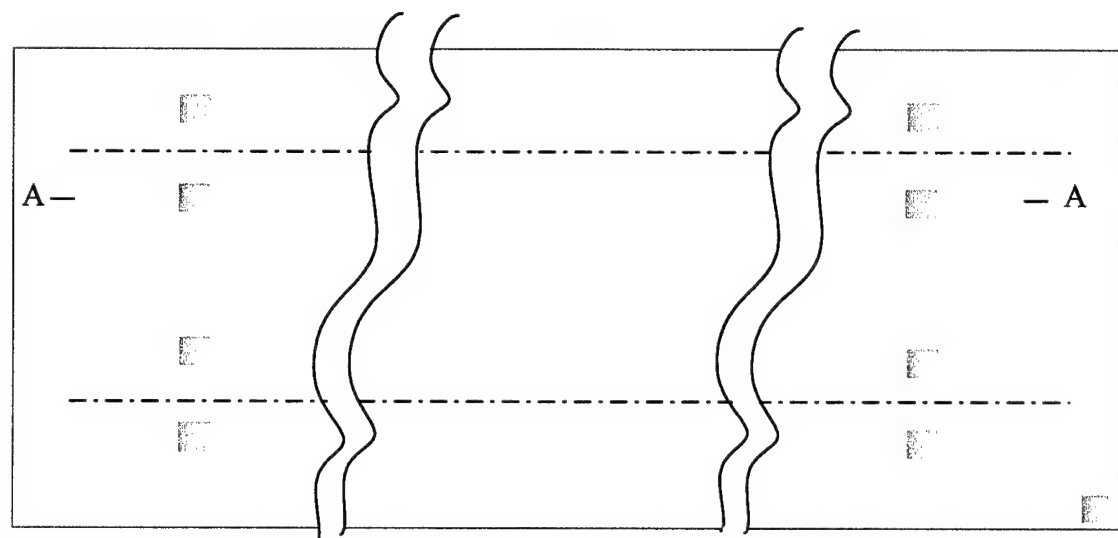
to avoid excess diffusion and 300MPa compressive stress



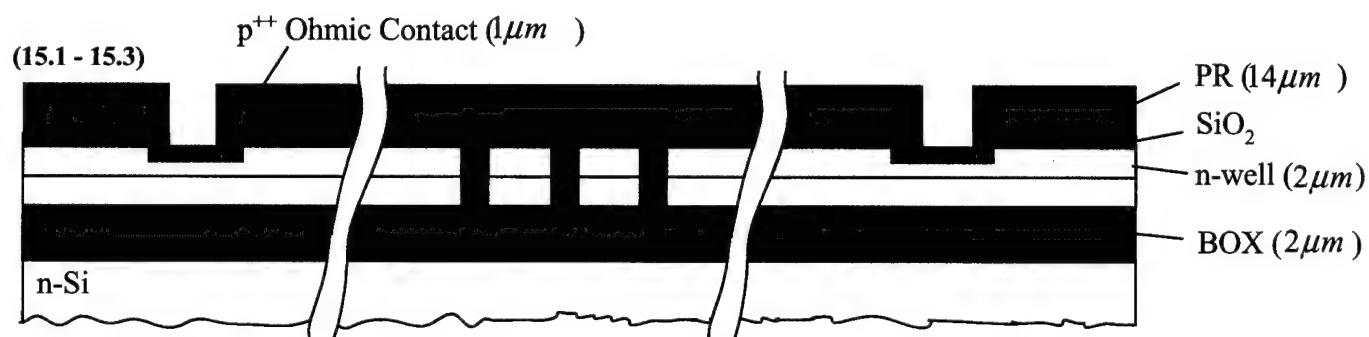
Bond Pads Cut

15.1	TRL/Coater	Spin photoresist on front surface, AZ9260, 0.25k/1k/3k, 6s/60s/10s, 12 μm Prebake, 95 C, 60 min
15.2	TRL/EV1	Pattern contact cuts using Bond Pads Cuts Mask (BPCM) Align to the alignment marks created by PCM . Expose for 45 sec (15*10*3) Develop, AZ440, 2 min 15 sec Postbake, 95 C, 30 min
15.3	TRL/Wet Bench	Etch oxide (BOE) Silicon as etch stop Create new alignment marks

(BPCM)

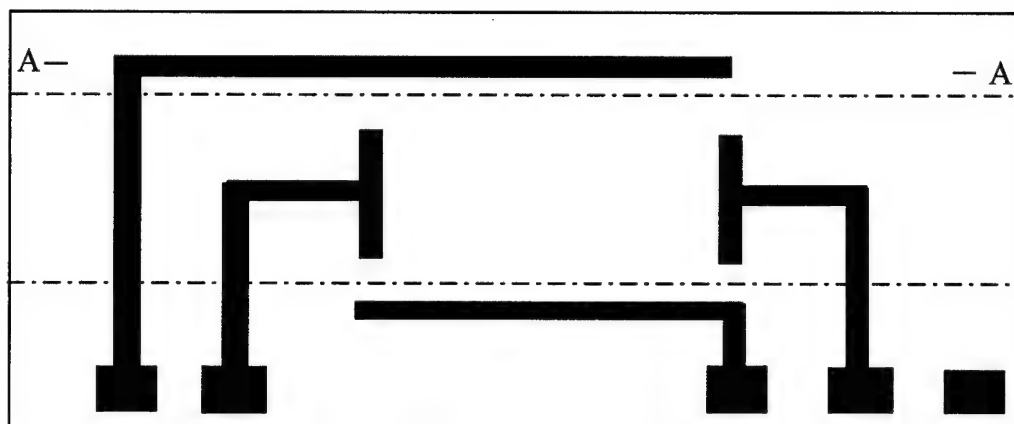


A - A



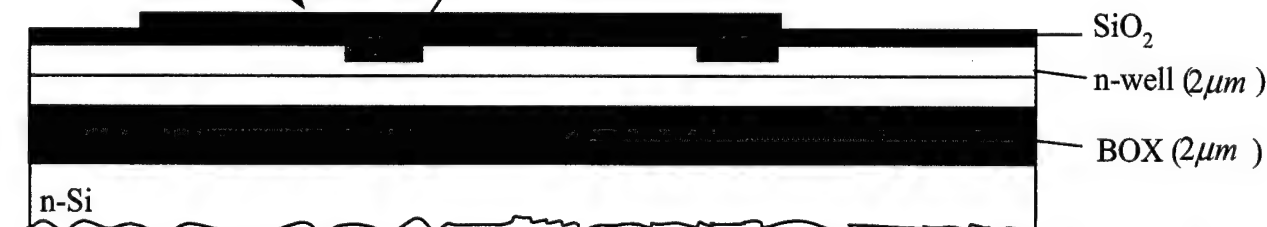
	15.4	TRL/Asher	Strip photoresist
Bond Pads	16.1	TRL/Coater	Spin photoresist on front surface, 7μm Prebake, 95 C, 60 min
	16.2	TRL/EV1	Pattern contact cuts using Shadow Mask (SM) Align to the alignment marks created by BPM . Prior expose Prebake, 100 C Flood expose Develop Postbake, 95 C, 30 min
	16.3	NPB/eBeam	Deposit 1 μm of Al-Si (1%) to avoid Al "spiking"
	16.4	TRL	Remove photoresist

(SM)



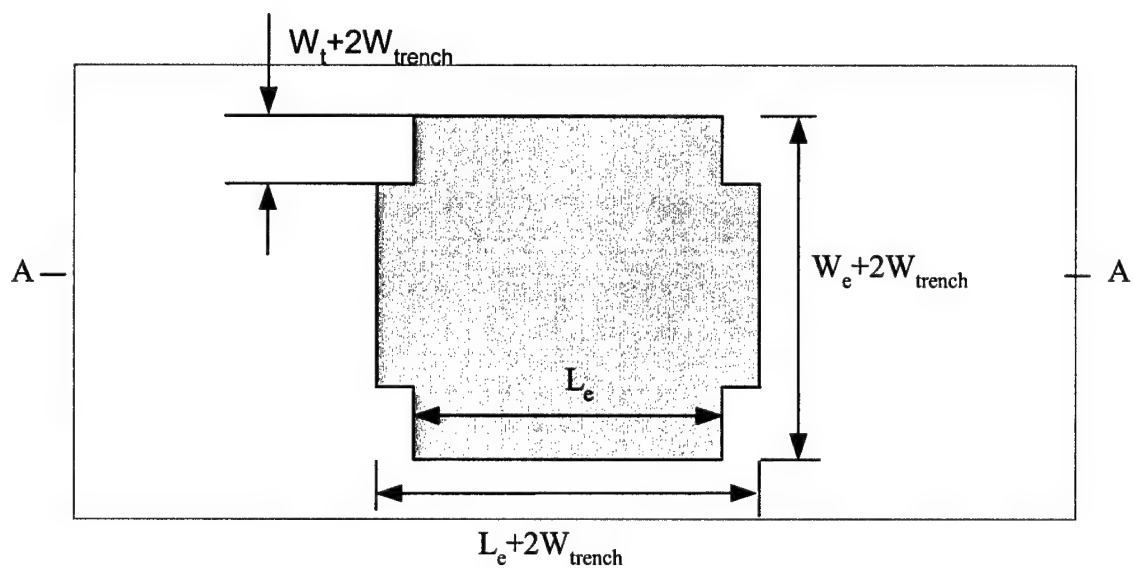
A - A

(16.2 - 16.4) Al-Si(1%)($1\mu\text{m}$) p^{++} ohmic contact ($1\mu\text{m}$)



Final Release	17.1	TRL/Coater	Spin photoresist on front surface, AZ9260, 0.25k/1k/3k, 6s/60s/10s, 12 um Prebake, 95 C, 60 min
	17.2	TRL/EV1	pattern using Final Release Mask (FRM) Align to the marks created via NM Expose for 45 sec (15*10*3) Develop, AZ440, 2 min 15 sec Postbake, 95 C, 30 min
	17.3	TRL/Wet bench	HF sacrificial oxide layer etch to release the floating element
	17.4	TRL/Asher TRL/Wet bench	Strip photoresist Pirahna clean

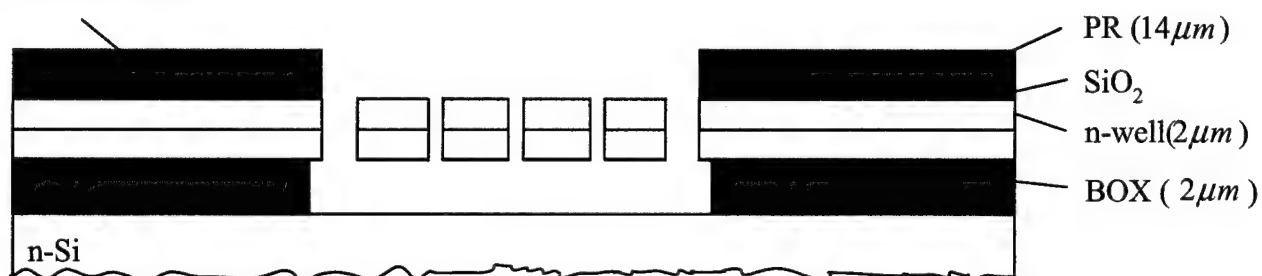
(FRM)



(17.1 - 17.3)

A - A

Al-Si(1%)($1\mu m$)



9 APPENDIX B

9.1 Fabrication Process Flow for Moiré Interferometry-Based Floating Element Sensor

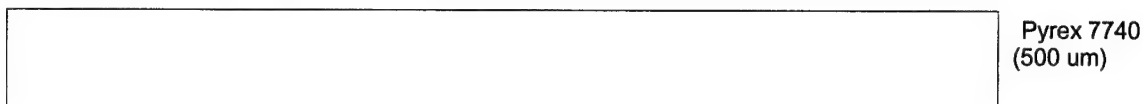
The following describe the process flow of the sensors.

Wafer

H	Handle	4" Corning 7740 glass (Pyrex) wafers 500µm thick
D	Device	4" p-type <100> 537.4 µm SOI wafers -- 12µm on top of BOX (0.4µm)
B	Bonded	handle and device wafers bonded front to front

Wafer Step Lab/Equip Process Description

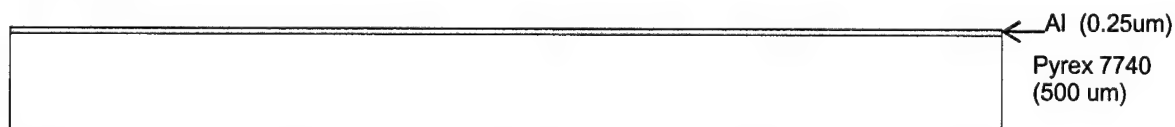
H 0
STEP 0 Begin with Pyrex Wafer



H 1.1 SNF Piranha clean (3:1 H₂SO₄ : H₂O₂), time = 15 min
Immerse in the H₂SO₄:H₂O₂ solution for 10 min
Then, immerse rinse in beaker with running DI water for another 5 min

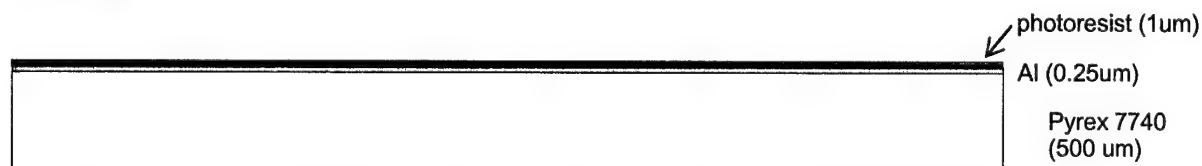
H 1.2 SNF Sputter Al (0.25µm)
Gryphon

STEP 1.1-1.2



H 1.3 SNF Spin 1 µm photoresist on top of Al coat
SVG Coater

STEP 1.3



H 1.4 SNF Pattern Photoresist
Sgvdev

MASK 1 - Handle Gratings, clear field

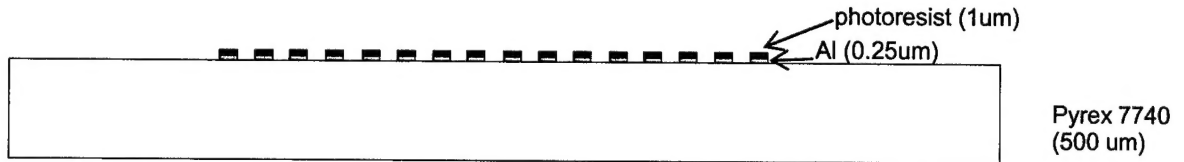
This mask will create two sets of alignment marks. The first set (left most) will be used to align the wafers for electrostatic bonding.

The second set will be used for the alignment of the mask for the final release-etch.

H 1.5 SNF Etch Al (H₃PO₄ : HNO₃) for 2min and a half (etch rate of 100nm/min at room temp)

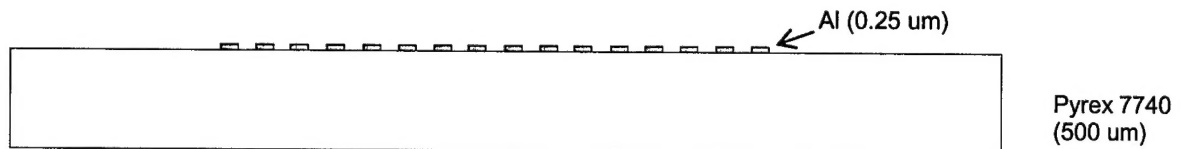
Wbmetal (This step is PAN etch)

STEP 1.4-1.5



H 1.6 SNF Ash resist

STEP 1.6

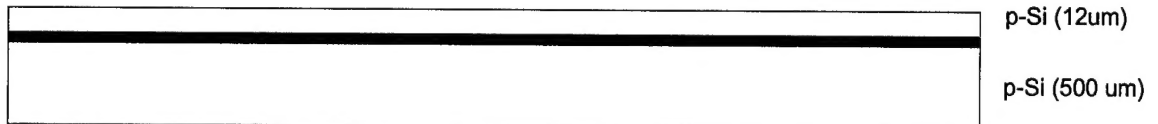


D 2 SNF Begin with 4" UNIBOND SMART CUT SOI wafer (p-Si FZ <100>, 14-22 ohm-cm) with 12 μ m Si on top of 0.4 μ m BOX)

Note: SOI wafer was fabricated using bonding of an active wafer p-type, FZ <100>, 14-22 ohm-cm and a handle wafer, p-type, CZ <100>, 14-22 ohm-cm (substrate thickness of 525um)

D 3.1 SNF RCA clean

STEP 2-3.1



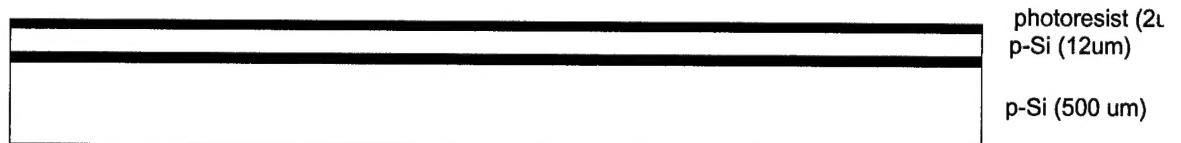
D 3.2 SNF Spin 2 μ m photoresist

SGV Coater

D 3.3 SNF Pattern photoresist

Sgvdev

STEP 3.2-3.3



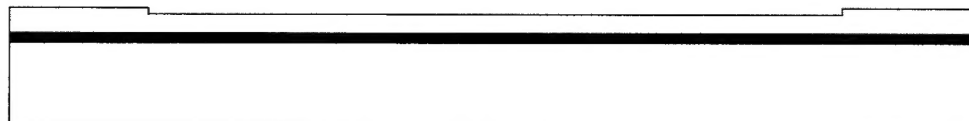
MASK 2 - Device Gratings Recess, dark field

D 3.4 SNF RIE Etch Si (2 μ m)

Note: RIE provide slower etch rates which will lead to smoother surfaces. Do dummy wafers

D 3.5 SNF Ash Resist
Use an O2 Plasma asher

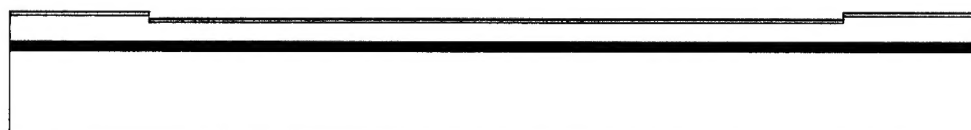
STEP 3.4-3.5



0.4um BOX
p-Si (500 um)

- D 4.1 SNF Piranha clean (3:1 H₂SO₄ : H₂O₂), time = 15 min
Immerse in the H₂SO₄:H₂O₂ solution for 10 min
Then, immerse in beaker with running DI water for another 5 min
- D 4.2 SNF Sputter Al (0.25um)
Gryphon Note: No step coverage.

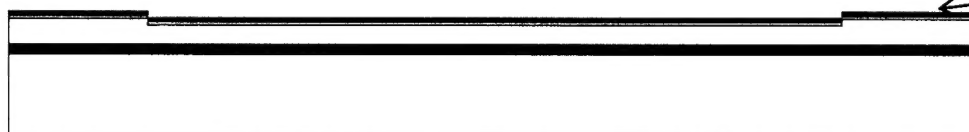
STEP 4.2



Al (0.25um)
0.4um BOX
p-Si (500 um)

- D 4.3 SNF Spin 4 um photoresist
SGV Coater
- D 4.4 SNF Pattern photoresist
Sgvdev

STEP 4.3-4.4



photoresist (4um)
Al (0.25um)
p-Si (500 um)

MASK 3 - Device Gratings, clear field

- D 4.5 SNF Etch Al (H₃PO₄ : HNO₃) for 2min and a half (etch rate of 100nm/min at room temp)
Wbmetal

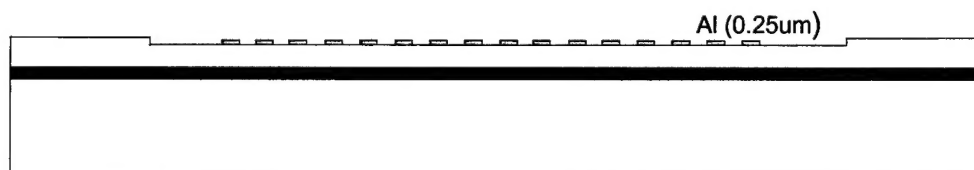
STEP 4.5



p-Si
0.4um BOX
p-Si (500 um)

- D 4.6 SNF Ash resist
Use an O₂ Plasma asher

STEP 4.6



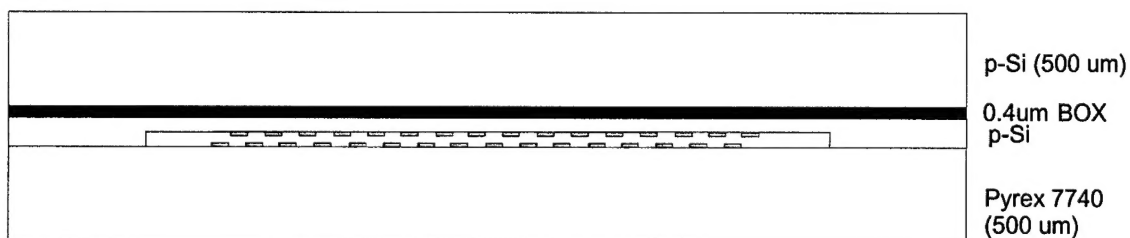
p-Si
0.4um BOX
p-Si (500 um)

- 5.1 SNF Clean Device and Handle Wafers using Standard metal clean (SNF specific clean)
 Wbmetal Put wafers in PRS1000 for 5 min
 Dump rinse wafer (120s) and spin dry (280s)
 Repeat rinse and dry sequence

Note: Do Handle and Device wafers separately.

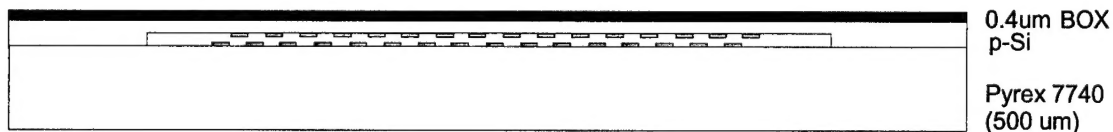
- B = D 5.2 SNF Low Temp Electrostatic Bonding (Please refer to attached diagram for setup)
 +H
 501 Wafer **Alignment is critical.**
 Bonder Use the EV anodic bonder and do a back side alignment of the Pyrex and the
 SOI wafers.
 Refer to Stanford recipe for the EV anodic bonder.

STEP 5.2



- B 6.1 UF Etch Si Device Wafer down to the insulating oxide using KOH (65C)
 Wbgeneral Protect backside with black wax or carnuba (depending on method used)
 Etch stopped on buried oxide.

STEP 6.1



- B 6.2 UF Clean wax from backside
 B 6.3 UF Post KOH clean
 Rinse with DI water, time = 10min, dry in N2.

- B 7.1 UF Coat backside with resist (2 μm)
 B 7.2 UF Etch 0.4 um of SiO2 using HF
 B 7.3 UF Ash resist

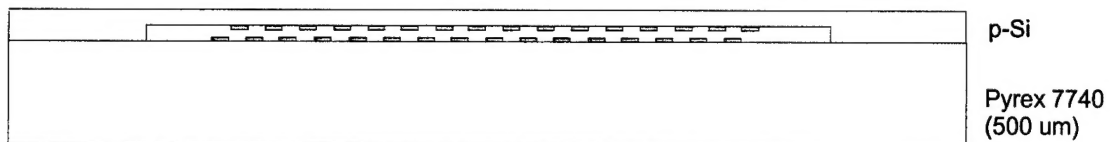
- B 8.1 SNF Spin 2 μm Photoresist
 SGV Coater

- B 8.2 SNF Pattern Photoresist
 Sgvdev

MASK 4 - Floating Structure Release, dark field

Alignment is critical. This mask needs to be aligned to the ones on the top of the Pyrex using back side alignment.

STEP 6.2-8.2



B 8.3 SNF DRIE to etch Si to release structure (10 μm)
STSEtch Etch rate of Si is 5 $\mu\text{m}/\text{min}$ with selectivity Photoresist to Si 75:1

B 8.4 SNF Ash resist using **plasma** asher

STEP 8.3-8.4

